Variant Parameters effect on OFDM Estimation Power Consumption

Sameer Al-Obaidi, M. Ambroze, N. Outram, B. Ghita

***Abstract*—Reduction power consumption is the goal of the next generation networks. This types of networks targeted Orthogonal Frequency Division Multiplexing (OFDM) as a main modulation technique due to properties of high spectral efficiency, high transmission speed and versatility. But its suffers from high power consumption due to computational complexity and complex digital signal processing. Many factors are effect power consumption OFDM and junction temperature such as cyclic prefix, Fast Fourier transform/Inverse (FFT/IFFT) Bit precision and transform length. In this paper introduce a method to analyses a power consumption for IFFT/FFT in OFDM design in detail. It is an important point to find a method to estimate power consumption and reduce it in the future. In addition; exploring estimation power consumption method affected by the length of IFFT/FFT using special tool from Xilinx.**

***Keywords*— Kintex-7 FPGA, OFDM, Xilinx power estimation, IFFT Transform Length.**

I. INTRODUCTION

The power consumption is a big challenge of the next generation networks due to increasing network capacity which support bandwidth-hungry application such as mobile networks, cloud computing and high resolution video. Therefore, our world is dominated by network, and the best step toward the greener world is reduced power consumption of modulation in the electronic network devices. many method is used to reduce power consumption as described in review paper [1]. OFDM modulation techniques is targeted next generation networks promising techniques due to high capacity and flexibility, but it is suffering from high consumption power [2]. This occurs because the mathematical operation of complex digital signal processing so it's the negative point which effect OFDM. The most power consumption is derived by IFFT/FFT block because digital signal processing operation of mathematical operation occurs inside it [3]

This paper explores a method to estimate OFDM power consumption in IFFT/FFT during design cycle. In addition, present the effect of IFFT/FFT transform length on power consumption design model.

II. XPOWER ANALYSES METHOD

Reduction of power consumption and increased network capacity is the main goals of next generation networks. One of the most modulation schemes for that purpose is OFDM modulation. This technique includes IFFT/FFT as a central mathematical base operation and it consumes a lot of power when compared with other parts such as Modulation/De modulation, serial to parallel and DAC/ADC due to a mathematical operations and complex digital signal processing [4]. The estimation power consumption of the OFDM transceiver FPGA design model is achieved by using special tools supported by Xilinx. This uses to estimate On chip power and junction temperature specification of FPGA during any stage of the design cycle such as pre-design and pre-implementation. Xilinx provide Power Estimation [XPE] Excel spreadsheet [5]. This includes Memory interface, Quick estimate, Transceiver configuration and memory generator wizard.

III. MODEL DESIGN IMPLEMENTATION

OFDM design model is implemented in Xilinx KC705 high speed analogue evaluation board which designed by Avnet [6]. This board integrated with DAC/ADC connected through FPGA Mezzanine Card (FMC) connector. In design cycle stage Xilinx provide a Simulink tool joint with Matlab 2012b and using Xilinx ISE14.7 system generator. In system generator stage it applicable to simulate the design and view the signal in each stage before implementation. The block diagram of the OFDM design model as in Figure (1) including Digital to Analogue/Analogue to digital convertor (DAC/ADC). This model starts from data Modulation using Quadrature Phase Shift Keying (QPSK), serial to parallel with specific length input to IFFT, Inverse fast Fourier Transform with option to add cyclic prefix and it is the main part of OFDM.

The first step to estimate power [7]as in Figure (2) show the system generator block with an option of Timing and Power analyses. Firstly, define the board type for this design through the Xilinx system generator block by selecting Kintex-7 xc7-325t-2 ffg900. Secondly, select generate and click on it generate power report of the design model. The setting option includes the type of power analyses used in our design select option quick analyses.

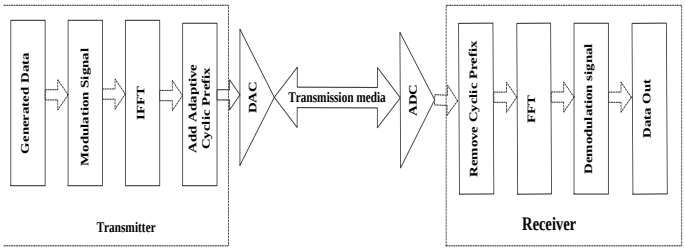

Fig. 1. OFDM block diagram

Sameer Al-Obaidi, M. Ambroze, N. Outram, B. Ghita are with Plymouth University, United Kingdom

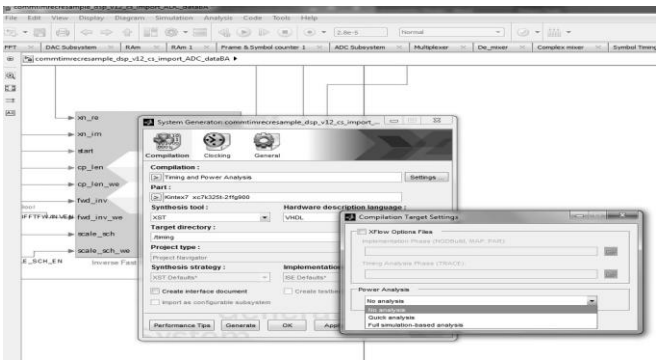

Fig. 2.System Generator Compilation target setting

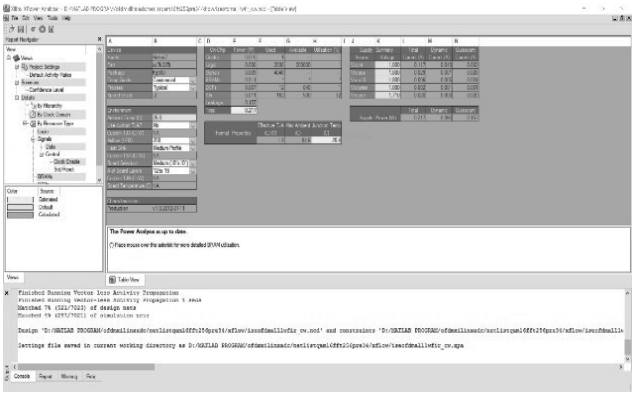

Fig. 3. Xilinx power consumption report.

The result output is the timing analyses constraint report as in figure 4. This report includes all information data needed about the design implementation and generate the power analyses report. The output generated report includes total power, thermal power and hierarchy power which means a power estimation for each part of the design including signal power as in Figure (4). In addition; It is included the power of functional logic, supply voltage, and On Chip Junction temperature.

The Xilinx Power Estimation XPE file is generated from the report above by select file menu and Export result to XPower Estimator XML Data (XPE) file. It is used in Excel spreadsheet to analyse power consumption and supported by Xilinx as in Figure (5). The generated advance power is used in next section for analyse power. This is represented the power estimation as a graph for On-Chip Power by function logic, Maximum power and junction temperature with static current by supply voltage as in Figure (6).

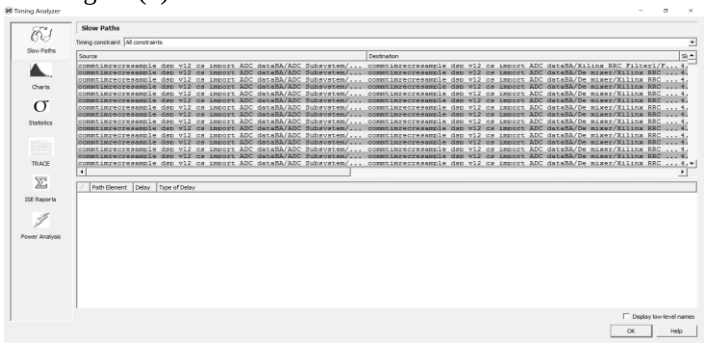

Fig. 4. Timing Analyses

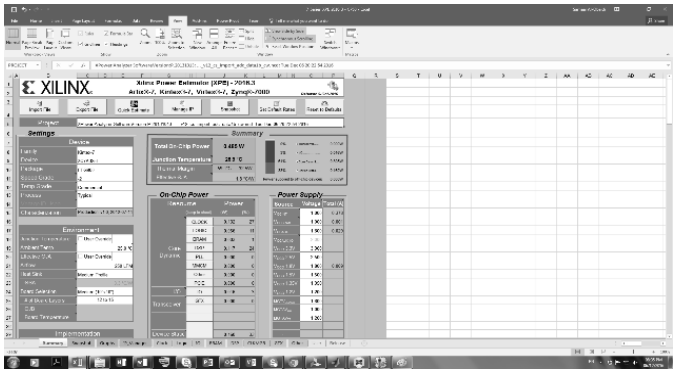

Fig. 5 . Excel spreadsheet to estimate power

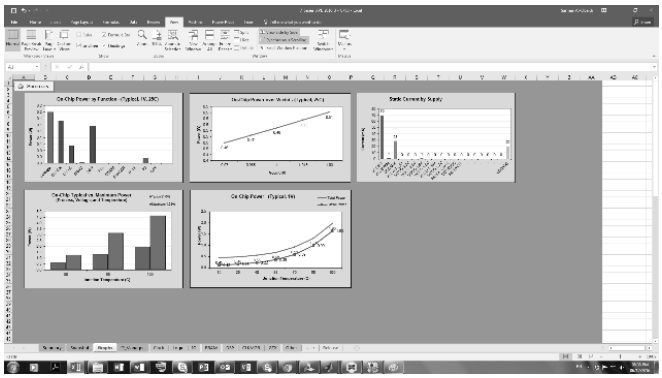

Fig. 6. Power graph with junction temperature.

IV. IFFT/FFT LENGTH EFFECT POWER CONSUMPTION

Next generation high speed multicarrier modulation is used OFDM as a base modulation technique [9]. This technique is targeted by next generation networks. The main part of this technique is IFFT/FFT[8]. The input of this part is the parallel modulated signal and the output is OFDM modulated signal. The length of IFFT can be identify by depends on the length parallel input signal stored in RAM. The procedure to estimate power consumption described in previous section is applied in this experiment. In our experiment explore the effect of IFFT/FFT length in power consumption with relation to the On-Chip junction temperature. In this model design QPSK modulation is used with comparison two length types of IFFT (256, 512) points. the connection block of the IFFT as in figure (7). The configuration of IFFT is the Cyclic prefix 25, precision 8 bits and types pipelined as in figure (8).

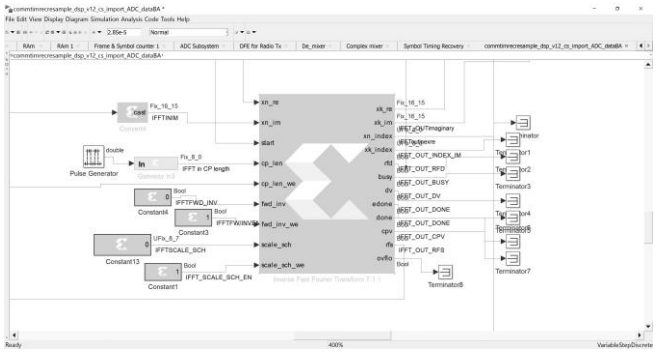

Fig. 7. Fast Fourier Transform connection

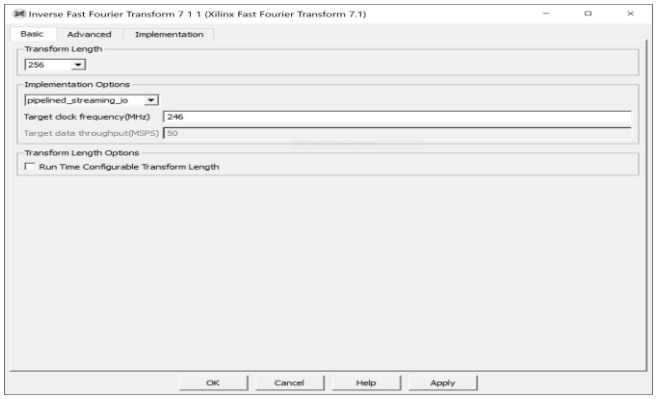

Fig. 8. Configuration IFFT

Fig. 9. IFFT Input/ Output signal Wave scope

The wave scope Input/ Output waveform of IFFT as in Figure 9 shows that 7 symbols per frame each symbol including 256 subcarriers modulated by QPSK. The controller of IFFT generate start signal to start processing of IFFT after the Ready for Start (RFS) is active high [9].

The power estimation of the design model is calculated through the system generator Matlab2012b. This version of Matlab is compatible with Kintex-7 high speed analogue evaluation board so the DAC/ADC can be simulated using Gateway (Out/In) block with option of DAC/ADC. Firstly; the program is run in Matlab then synthesis, mapping, Place and Route, timing and finally generate power report of the design model. The result generates a power report Xilinx XPower analyser as described in previous section and includes in detail the power of each part by hierarchy. The estimation power result of 512 point IFFT is (27.96mw) and FFT (26.16mw) as shown in Figure 10 compared with (23.55mw) for 256 point IFFT and FFT (22.63mw) as in Figure11. Therefore, the result shows the power consumption is increased when the length of IFFT/FFT is increased. In addition, power is consumed by IFFT/FFT is higher than the other parts in the design model that's approve the most power consumption part.

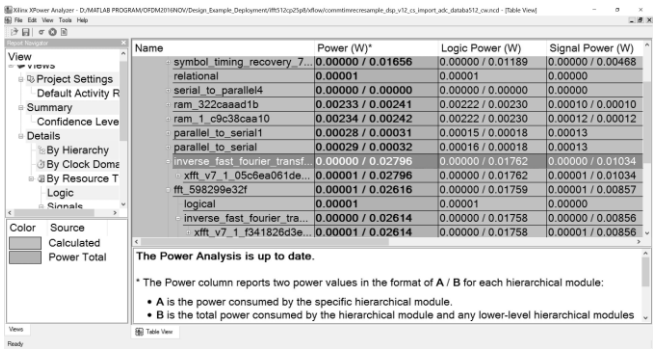

Fig. 10. 512 IFFT/FFT Estimation Power Consumption

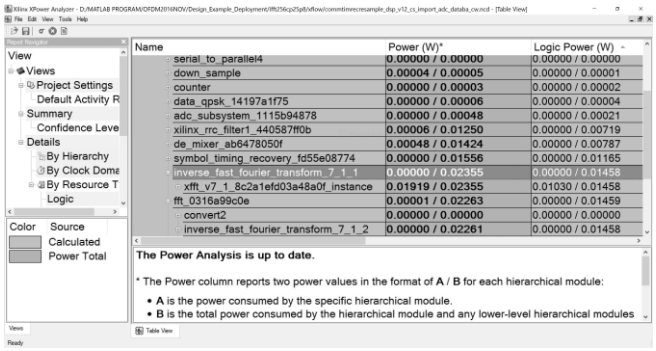

Fig. 11. 256 point IFFT estimation power

The file generate a Xilinx power estimation file (.XPE) is used in next step with spreadsheet to find the On-Chip junction temperature. The spread sheet shows the summary of power estimation for the OFDM design as in Figure 12. This represent the power consumption of 256 IFFT/FFT and includes the information about the board temperature, power and source voltage. The spreadsheet imports the (.XPE) file generated from previous figures (10,11). In addition, changing some parameter such as fan speed or ambient temperature, process type to maximum led to changing in On-Chip power. The summery page of Excel spread sheet when increasing length of IFFT/FFT to 512 led to increasing power as in figure (13). The summery worksheet tab includes all information about the design when implemented in FPGA for specific Evaluation board.

Fig. 12. 256 IFFT spread sheet

Fig. 13. 512 point IFFT/FFT Summery tab power estimation

The comparison of On Chip Power information in spreadsheet of IFFT/FFT (256/512) figures (12,13). Firstly; On chip power is increased for logic, DSP and I/O due to increase size of IFFT/FFT so need more mathematical operation and more spaces in FPGA.

The Xilinx power estimation represented as a graph in spreadsheet and contain an option for On-Chip junction temperature. The analyses of junction temperature show that (0.48w) for 256 point IFFT which increased to (0.55W) for 512 point at 25 °C as in figures (14,15)

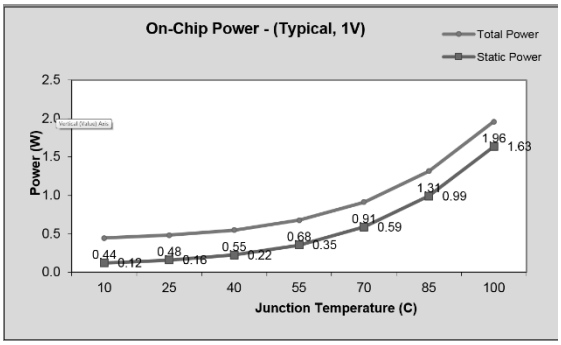

Fig. 14. On-Chip Junction Temperature 256 IFFT/FFT

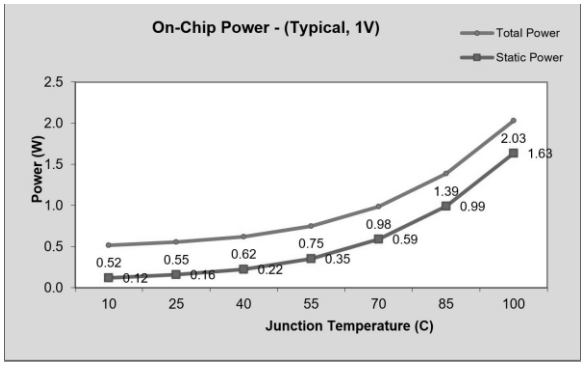

Fig. 15. On-Chip Junction Temperature 512 IFFT/FFT

In the analyses above shows that forward relation between power consumption and length of IFFT/FFT. However; when compare the data processing with period of time which means data transmitted with 512 point IFFT is twice the data with 256 point IFFT in the same period of time. Therefore; transmitted 3 frames of data with 7 symbols each symbol 256 subcarriers in period (2.5*10-5 sec). for 256 point IFFT. In the same period of time when using 512 point IFFT the transmitted same data by less than two frames. In conclusion the power is increased when increased in length of IFFT/FFT but can processing double the data with small difference of power.

V. Conclusion

Main goal of next generation networks is reduced power consumption towards a green world Networks. However; OFDM modulation is targeted as the main modulation for this type of network. Therefore, the previous analyses in this paper focus on estimate power consumption of one main part IFFT/FFT of OFDM. The procedure to estimate power consumption described in previous section through this paper it is like a novel for study by using tools from Xilinx for analyses. During the study is found that forward relation between length of IFFT and power consumption. In addition, the power increased when increasing number of parallel data input to IFFT/FFT but the data input is increased that mean more data can be processing when increased length of IFFT/FFT.

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Sameer. Al-Obaidi. Received his B.SC 1997-2000 and M.SC2000-2003 from Electronics and communication engineering department/ Al-Nahrain University/ Baghdad/Iraq. He is employed as a lecturer at Baghdad University from 2008. Now do a research to complete Ph.D. in Electronic and Communications at Plymouth University/Centre for Security, Communications and Network Research (CSCAN). In addition, he was a member of IEEE communication society.