Analysis of Double Gate Tunneling FET characteristics for Low Power Designs Suppression

S.M. Turkane, and Dr.A.K.Kureshi

***Abstract*—** The continuous down-scaling of MOSFETs gives faster and more complex chip design. As the devices scale down, supply voltage should be decreased accordingly. However the reduction in power consumption of MOSFETs is becoming increasingly difficult. The reduction of MOSFET size causes high sub-threshold swing, leakage current (I_{off}) and short channel effect. In this paper Tunnel FET (TFET) is studied as alternative device which could overcome physical limits of MOSTETs. TFET is simply a gated p-i-n diode. TFET works on the principle of band to band tunnelling. TFETs do not suffer from short channel effect and it has small sub-threshold swing and low off current. This paper introduces and summarizes progress in the development of the tunnel field-effect transistors relative to the metal–oxide–semiconductor field-effect transistor, design trade-offs, and fundamental challenges.

***Keywords*—**Application-Specific Integrated Circuits (ASIC), Area comparison, Delay comparison, Field Programmable Gate Array (FPGA).

I. Introduction

A. MOSFET and CMOS Technology

FOR long battery life devices low supply voltage is required as active power is proportional to square of voltage. In CMOS, low input voltage shows degradation in performance due to dependency of drive current on threshold voltage thus CMOS technology is limiting in low power region [6].

We are scaling the MOSFET and CMOS devices for further optimization & energy conservation. But now technology has reached its optimum limit. This is because, scaling down is limited due to certain constraints like power dissipation, degradation in switching performance etc. Sub-threshold swing of MOSFETs is limited by 60mv/decade. As MOSFETs are scaled down power supply voltage should be scaled down to reduce power dissipation. But reduction of power dissipation is difficult because of high sub-threshold swing, leakage current and short channel effect in scaled MOSFETs. Reduction of MOSFETs, CMOS ICs shows good switching speed, functionality and lower cost of chips. There is main problem in scaling that is high power consumption; the difficulty in reducing power supply voltage; higher leakage current.

Tunnel field effect transistor (TFET) is one of the alternatives to MOSFETs replacement, which is work on the principle of band to band tunnelling. TFETs give smaller sub-threshold slope below 60mv/decade at room temperature. This gives lower cut off current and smaller leakage power. As per literature survey ON currents of TFET very lower than MOSFETs this is unaccepted .according to ITRS (International Technology Road for Semiconductor) Tunnel FET is one of the possible transistor option for ultra-low power designs[7,8,10].

TFET is good option for low power logic applications it performs faster than CMOS at around 0.3V supply voltage. TFET is based on quantum mechanical effect i.e. tunnelling [6].

B. Scaling Rules

There have been proposed several sets of rules for scaling, for the purpose of discovering as much as possible the electrical consequences of MOSFET size reduction. Principle among these are rules by Dennard in 1974 (1 μm channel length) [1, 2, 3].

By scaling, we hope to

- Increase packing density
- Increase Functionality of chip.
- Increase current of devices and speed also.
- Lower cost of devices.

But the trade-offs are

- Short channel effect.
- Higher leakage current.
- Sub-threshold swing limited to 60mV/decade.

One of the device people are looking at, to overcome SCEs of MOSFET is the Tunnel Field Effect Transistor (TFET).

II. Tunnel Field Effect Transistor

In this section we explain the working principle of the device. The basic principle of operation of the device is based on the band-to-band tunnelling mechanism. In TFET band to band tunnelling occur between valence band of p-region and the conduction band of an n-region. Introduces an ultra-low power asynchronous self-timed design methodology for brain-machine interface systems as an attractive alternative for the realization of robust and energy-efficient computation.

Satish M Turkane is working as an Associate Professor in Pravara Rural Engineering College, Loni and pursuing his Ph.D at Matoshri College of Engineering & Research Centre, Eklahare, Nashik, Savitribai Phule Pune University, Pune, Maharashtra, India.

Dr.A.K.Kureshi is Principal, Vishwabharti Academy's College of Engineering, Ahmednagar, Savitribai Phule Pune University, Pune, Maharashtra, India.

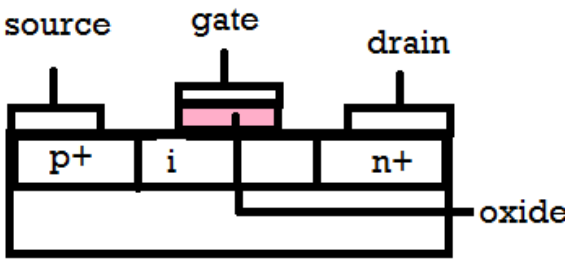


Fig.1 Basic structure of Tunnel FET

TFET is p-i-n structure which is reverse biased device. Fig.1 shows basic structure of TFET. Reverse biasing is takes place between drain and source terminal of TFET and gate controls the device current [8].

The N-TFET and N-MOS structure is shown in Fig.2 and Fig.3 respectively. NTFET has lightly n doped substrate. When a sufficient voltage is applied to the gate terminal of a TFET, formation of the inversion region in channel p+n+ tunnelling junction is formed. And hence electrons pass through the barrier and current flows through the transistor. In NMOS when high gate-source bias is applied electrons flow from the source to the drain. The corresponding energy band diagrams are shown in Fig.4 and Fig.5 respectively. Energy band diagram of NTFET shows that the electrons tunnel from the p+ doped region into the channel region and flow to the n+ doped region.

Tunnel FET is based on electron tunnelling and that, in principle, can switch on and off at lower voltages than the operation voltage of the MOSFET. Its use therefore is expected to reduce the power consumption of electronic devices. Because of this the current through the tunnel FET is smaller than the current through the MOSFET.

TFETs are suitable to conduct current in one direction. This characteristic referred to as unidirectional conduction. It causes significant challenge in the design TFET SRAM. Because the access transistors requirement of SRAM to conduct current in both directions. For SRAM cells, unidirectional characteristics severely impact robustness [11].

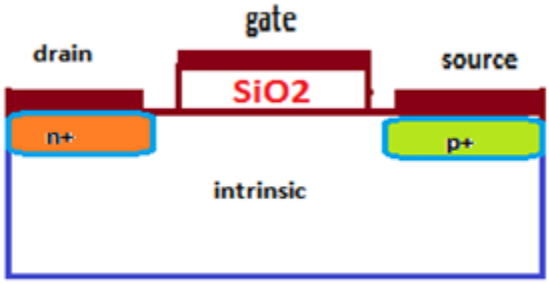


Fig.2. N-TFET structure

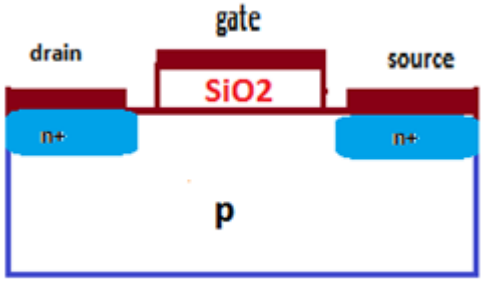


Fig.3 N-MOS structure.

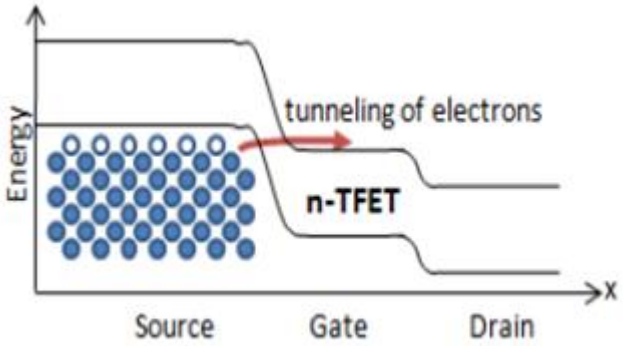


Fig.4 Energy band diagram of N-TFET

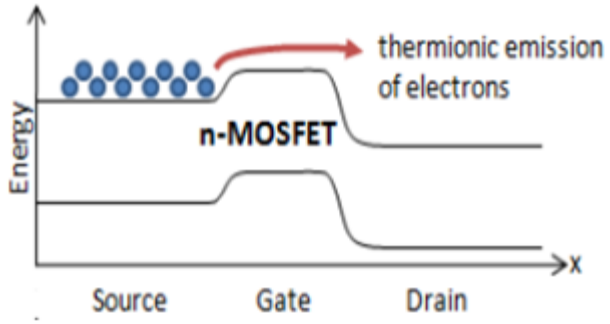


Fig.5 Energy band diagram of N-MOS.

2.1 Band-To-Band Tunneling

The scientists have claimed that by 2017, a quantum phenomenon known as the tunnel effect will help reduce energy consumption of consumer electronics by up to 100 times less than now [5]. In band to band tunnelling, electron in valence band tunnel across the band gap to conduction band. Fig.5 shows band to band tunnelling mechanism.

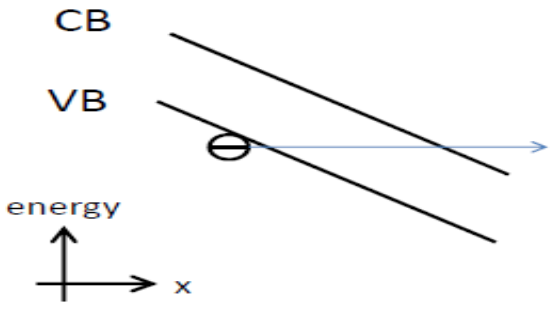


Fig.6 Band to Band Tunnelling

Two types of Tunnelling:

1. Direct tunneling: An electron moves from the valance band to the conduction band without the absorption or emission of photon in the direct tunneling.
2. Indirect tunneling: An electron moves from the valance band to the conduction band by absorbing or emitting a phonon in the indirect tunneling process.

III. Visual TCAD

We have used Visual TCAD, which is a simulator developed by to study, optimize and predict the behaviour of devices. TCAD is used to simulate devices to study characteristics like current, voltages carrier densities. It is useful simulation software to reduce the design costs, improve the device design productivity [9].

A. Core Components:

- Device Model Drawing
- Circuit Schematic Capturing
- Device Simulation Control
- Circuit/Device Mixed-Mode Simulation
- Visualization
- Text Editor
- Spreadsheet
- X-Y Graphs

The simulation engine behind Visual TCAD is designed to take advantage of parallel computers. With a 4-node, 32-core cluster, Simulation time is reduced by almost 10 times. Simulation of large device structures, such as CMOS circuit cells and SRAM memory cells has become practical. It also provides High Quality Mesh. The intelligent mesh generator produces adaptive and high quality mesh with little user tuning, and leads to faster convergence and more accurate simulation results.

IV. Device Structure And Simulations

In this work we focus on the performance analysis of double gate TFETs. The dimensions of device which are used for our simulations are as shown in fig.6. The channel length of 24 nm is used. The oxide thickness is 1 nm. The source and drain contacts are made of aluminium, and the work function of gate metal is 4.17 eV. Gaussian doping profiles, with a peak concentration of 10^{20} atoms/cm^3 and 5X 10^{18} atoms/cm^3 for the source (p-type) and drain (n-type) regions respectively. The channel region is made of a moderately doped 1 × 10^{17} atoms/cm^3 n-type layer. The results presented here are obtained by using a non-local Band to Band Tunnelling model combined with a band gap narrowing model.

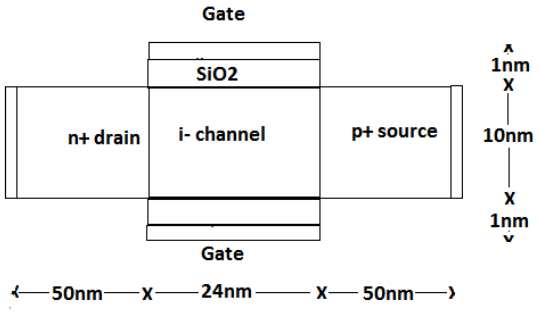


Fig. 7 Simulated n-TFET DG.SiO_2 thickness =1nm C_{hannel}= 25nm. Drain doping (n+) = 5X10^{18} atoms/cm^3 and source doping (p+) = 10^{20}atoms/cm^3

TABLE I
DEVICE PARAMETERS

Parmeter	Value
Channel length	25nm
Source doping	1X10^{20}atoms/cm^3
Drain doping	5X10^{18} atoms/cm^3
Substrate doping	1X10^{16} atoms/cm^3
Sio2 thikness	1nm
Body thikness	10nm
Work function of gate	4.3ev

A band to band tunneling model was used for tunneling. For current transport drift diffusion model is used.

V. Simulation Results

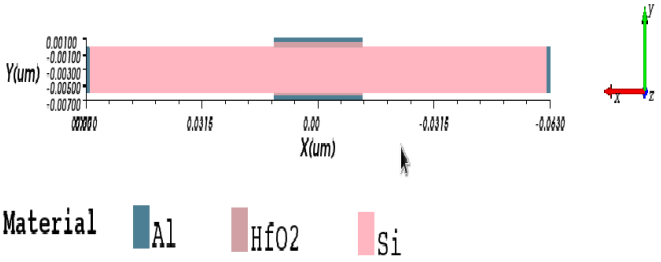


Fig.8 Material structer of DG-TFET

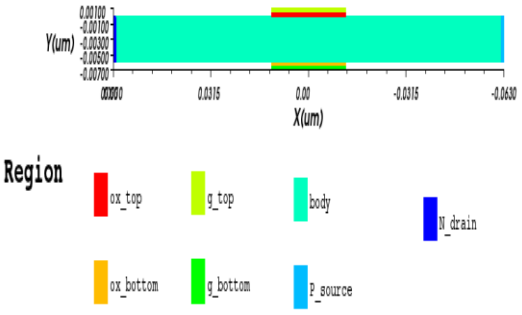


Fig. 9 Regions of TFET

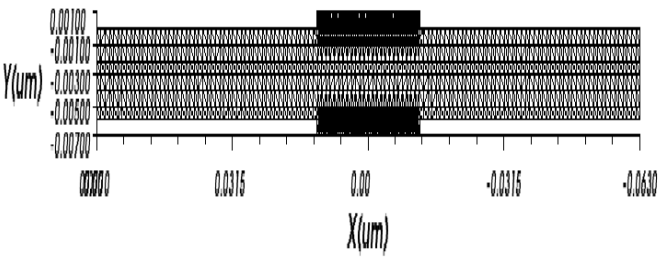


Fig. 10 Meshing of TFET

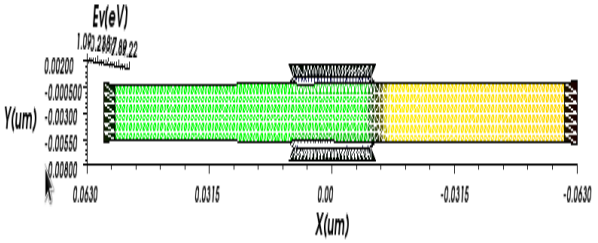


Fig.12 Valence band energy in TFET

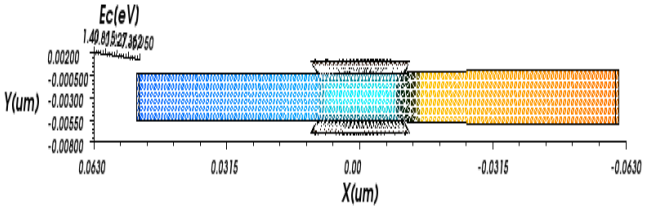


Fig. 11 Conduction energy of TFET

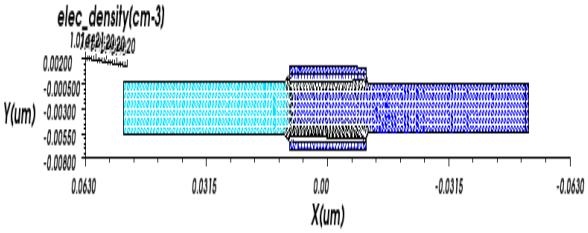
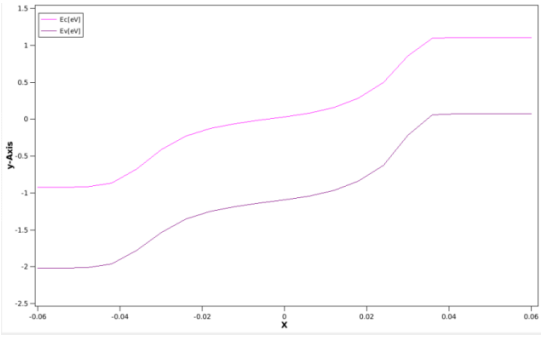
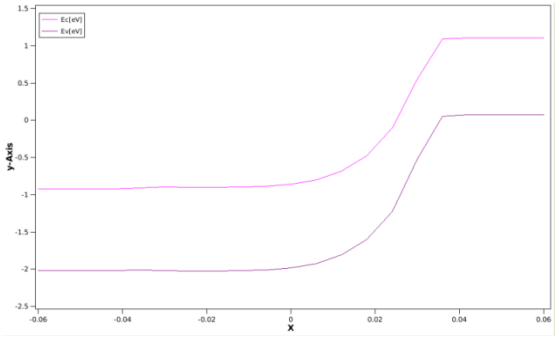


Fig.13 Electron density of TFET



(a)



(b)

Fig. 14 Schematic of energy band diagram of DG-TFET
(a)energy-band diag. of the OFF-state i.e.Vd = 1V & Vg =0V

(b) energy-band diag. of the ON-state Vd = 1 V &Vg = 1

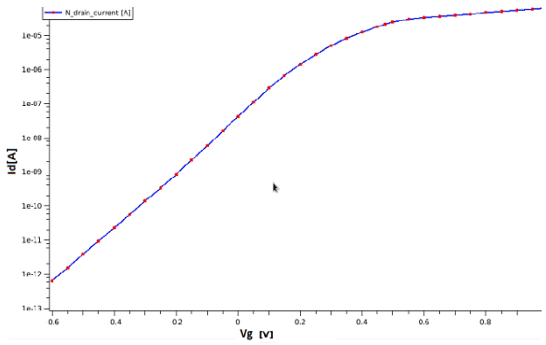


Fig. 15 Transfer characteristics of TFET

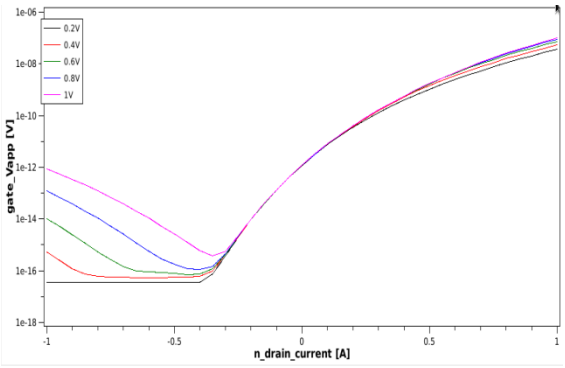


Fig. 16 DG-TFET Id-VG characteristics for different gate voltages

In Double gate Tunnel-FET, the current is doubled due to two gate voltage. Hence, the ON-current is larger than single gate TFET OFF-current is lower [4]. In TFET for different values of V_{ds} voltage and I_{off} is decreasing. Comparing this

with MOSFET, this is good achievement in energy saving in low power devices.

In this work, the physics of optimizing DG TFET performance is discussed. Strong gate coupling at the centre of the silicon film at the source is important for modulating the band-to-band tunnelling.

VI. Advantages

TFET have no. of advantages over MOSFET:

1. Applicable to the low power application.
2. The low leakage current.
3. The tunneling effect enhances the device operating speed.
4. Small threshold voltage as it depends on the band bending tunnel region, not on the channel region.
5. Absence of short-channel effects (SCE)
6. Low off-currents.
7. No punch-through effect.
8. Lower sub-threshold slope.

VII. Conclusion

In this work, performance of TFET is discussed. We proposed and discussed the basic static operation, and studied by simulation the characteristics of a DG Tunnel FET as a better-than-60-mV/dec current switch. Tunnel FET has lower sub-threshold slope than MOSFETs. Tunnel FET is applicable for low power devices as it gives lower off currents. It is difficult to achieve high *ION* without degrading *IOFF*, and sub-threshold slope below 60mV/dec.

Also the unidirectional conduction characteristic is causes a challenge in design of logic devices such as SRAM and pass transistor logic.

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