

# Study of Fully Depleted DUAL MATERIAL GATE (DMG) SOI MOSFET at Nano Domain

Ashwani Rana, and B.H.V Shrikant

**Abstract**—The scaling of MOS devices down to 25nm regime has brought our focus to Short Channel Effects. This has also led us to try some new devices which can perform well at technologies like 25nm. DUAL MATERIAL GATE MOSFET is one such device. In this paper, we have analyzed DMG MOSFET by varying dielectric constant of spacer material. We observed that best results are obtained when HfO<sub>2</sub> is used as spacer material. We also observed that for L1:L2 = 1, the device performance is better than any other ratio. The effect of variation of gate oxide thickness and work function difference of the two gate metals is also studied to optimize the device.

**Keywords**—DIBL, FD SOI DMG and SMG MOSFET,  $I_{on}/I_{off}$ , SCE, TCAD.

## I. INTRODUCTION

THE Dual Material Gate MOSFET incorporates the concept of laterally amalgamated metals which are used to form the gate of the MOSFET. These metals have difference in their work functions. For an n-channel MOSFET, the workfunction of the metal used in the source side is higher than the workfunction of the metal used in the drain side and vice versa for a p-channel MOSFET. This creates a step in the channel potential. This paper is a study of performance improvements of DMG MOSFET and its effective suppression of the short channel effects in FD SOI MOSFETs. The Dual Material Gate structure was first proposed by Long [2] in 1999. Gate material engineering was used instead of doping engineering [3-6]. When we are using gate material engineering, the channel potential is redistributed in such way that the short channel effects are reduced and transport of carriers is enhanced. A similar concept was first proposed by M. Shur [1] by applying different gate bias in split-gate structure. But there was a problem of fringing capacitance which made it difficult to realize the two metal split-gate FET. As the distance between the two metal gates decreases, the fringing capacitance of the split-gate FET increases. There is a way of fabricating Hetro-Material Gate Structure by inserting one additional mask in

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the bulk CMOS processing technology which was first suggested by Zhou [7]. He also showed the characteristics of this new structure.

## II. SHORT CHANNEL EFFECTS

Due to the extent of integration getting more and more, it is important to reduce the modern VLSI's power consumption. This power consumption may be reduced by using a lower power supply voltage. But, by doing so, the current driving capability will get degraded. Thus, there is a strong need of scaling MOS devices in order to improve the current driving capability so that we can fabricate VLSI chips with improved functionality [8]. If the channel length of a device is reduced, the threshold voltage of the device reduces. This dependence of device characteristics on channel length is a Short Channel Effect (SCE) due to which there is a variation in the device characteristics due to variation in the channel length during manufacturing. This also affects the controllability of the gate voltage over the channel and hence drain current. Thus, the subthreshold slope of the device gets degraded and there is an increase in the drain off-current as a result of increase in leakage. There are some popular ways of preventing SCEs like using shallow source/drain junctions and thinning gate oxide [13].

While scaling down the device, if the channel length is of the order of channel depth, then SCEs occur. When we scale down the device, channel length is reduced which reduces the threshold voltage and hence degrades the control of the gate voltage over the channel due to increase in the charge sharing effect from source/drain. The first SCE model proposed by Poon and Yau [9] describes the charge sharing effect by gate and drain electric fields in the depletion channel.

When the device is operating in the weak inversion mode, there exists a potential barrier between the source and the channel which the electrons have to cross before entering the channel. This barrier height should ideally be controlled by the gate voltage. But, due to DIBL (as indicated in Fig. 1), when we change the drain voltage, there is a change in this barrier height. If we increase the potential at the drain side, this barrier height gets reduced and more carriers enter the channel from source leading to an increase in the drain off-current of the device. Thus, due to DIBL, the drain voltage along with the gate voltage is responsible for controlling the drain current.

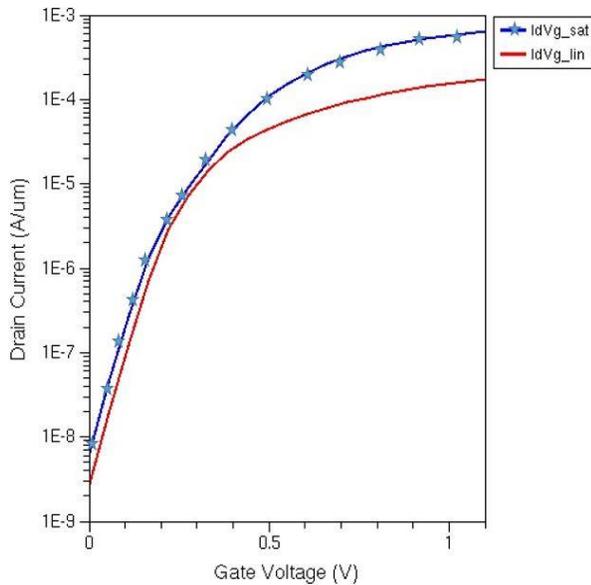


Fig. 1: DIBL Curve of SMG FD SOI MOSFET.

### III. DEVICE STRUCTURE

The dual material gate FD SOI MOSFET structure is as shown in Fig. 2. As we are working at 25nm technology, the channel length is 25nm, the lengths of source and drain are 45nm. Source/drain thickness is 6nm. The thickness of buried oxide layer is 20nm. Half of the gate is made up of Molybdenum and half of the gate is made up of Manganese.

One half of the gate near the source side is made up of Molybdenum and the other half of the gate is made up of Aluminium. There is a reduction in hot carrier effect due to half of the gate at the drain side being made up of lower workfunction metal which reduces the peak electric field.

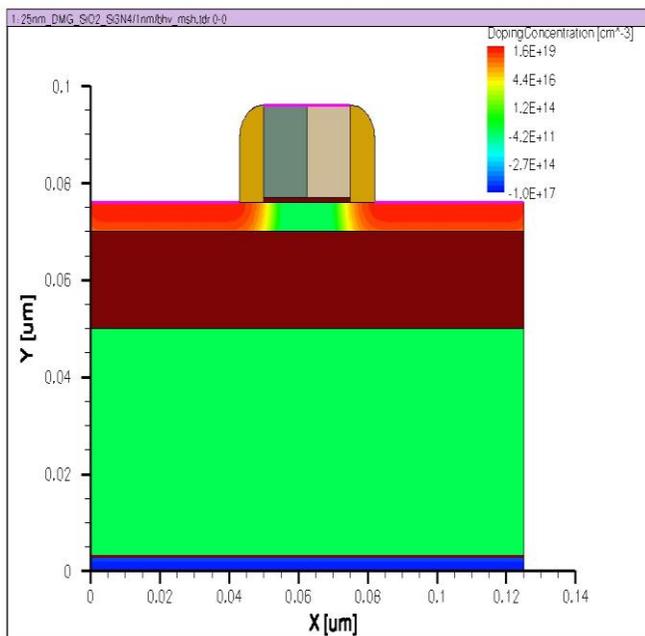


Fig. 2: Device Structure of DMG FD SOI MOSFET.

Also, there is an increase in the average velocity of electrons due to the half of the gate at the source side being made up of higher work function metal which enhances the peak electric field at the source side. Thus, in the dual material gate structure, there is an increase in transconductance and reduction in drain conductance.

### IV. RESULTS AND DISCUSSIONS

The DIBL curves for Single Material Gate Fully Depleted Silicon on Insulator MOSFET and Dual Material Gate Fully Depleted Silicon on Insulator MOSFET are plotted and the improvement in DIBL can be clearly seen from Fig. 3.

As explained earlier, there is a reduction in DIBL from 30.7 mV/V for SMG FD SOI MOSFET to 10.1 mV/V for DMG FD SOI MOSFET when  $\text{Si}_3\text{N}_4$  is used as spacer material. We have also studied and shown the effects of variation of dielectric constant of spacer material on  $I_{\text{on}}/I_{\text{off}}$  ratio (Fig. 4), DIBL (Fig. 5), Subthreshold Slope (Fig. 6) because when the dielectric constant of the spacer material is increased, the associated fringing electric field decreases. This reduction in fringing electric field is the cause for reduction in leakages.

We have varied the ratio of the lengths of the two gate metals (Fig. 6). The effect of variation of  $L_1:L_2$  on the device performance parameters are shown in Fig. 7, 8, 9, 10. The device is optimized for the ratio of the two gate metals as 1. Because, the surface potential minima occurs at the junction of the two metals used as gate material and keeping  $L_1 = L_2$  ensures that the surface potential minima is essentially at  $L/2$ , i.e., half of the channel length which results in better performance of the device.

Also, keeping  $L_1 = L_2$ , we have studied the effects of variation of gate oxide thickness as shown in Fig. 11, 12, 13, 14. The increase in gate oxide thickness increases the threshold voltage and reduces the gate tunneling leakage and hence the device performs better when the gate oxide thickness is kept 1.3nm. As the threshold voltage also increases with increasing gate oxide thickness, hence using thick gate oxide will make the device unsuitable for low power VLSI applications.

The variation of work function difference between the two gate metals is also studied and is shown in Fig. 15, 16, 17, 18. The more is the difference in the work function between the two gate metals, the more will be the screening of the source side from the effects of drain side and hence the device performance increases.

### V. CONCLUSION

It is concluded that the Dual Material Gate MOSFET performs better than the Single Material Gate MOSFET. We observed that when we are using the spacer material with high dielectric constant, short channel effects like DIBL and subthreshold slope are reduced and an increase in  $I_{\text{on}}/I_{\text{off}}$  is seen. Also, the device performance is best for  $L_1:L_2 = 1$  and the device is optimized for gate oxide thickness and work function difference between the two gate metals. Thus, DMG MOSFET is suitable for the VLSI application at 25nm nanometer regime.

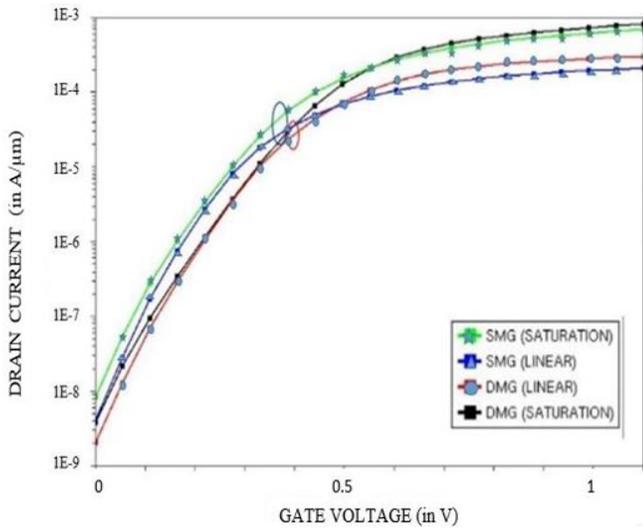


Fig. 3: Comparison of DIBL Curves of SMG and DMG FD SOI MOSFET.

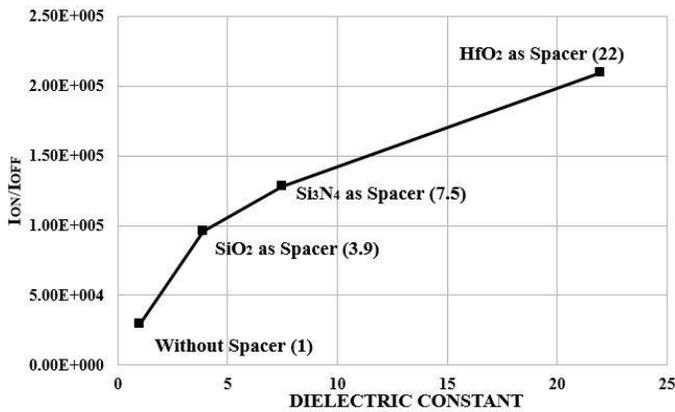


Fig. 4:  $I_{on}/I_{off}$  graph of DMG FD SOI MOSFET for different spacer materials.

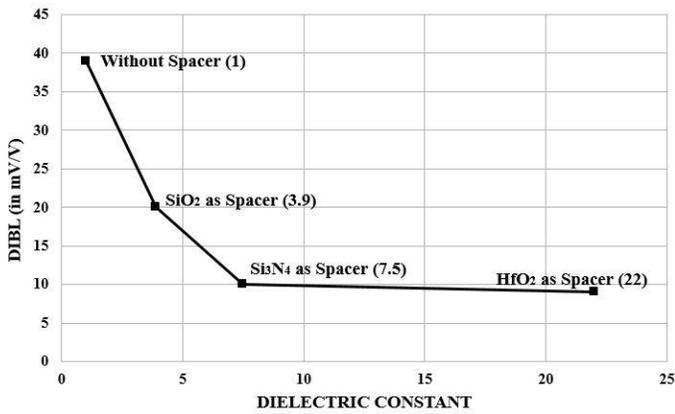


Fig. 5: DIBL graph of DMG FD SOI MOSFET for different spacer materials.

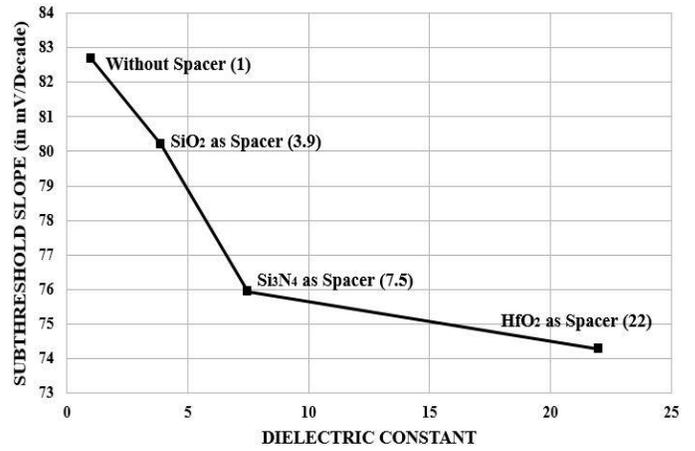


Fig. 6: Subthreshold graph of DMG FD SOI MOSFET for different spacer materials.

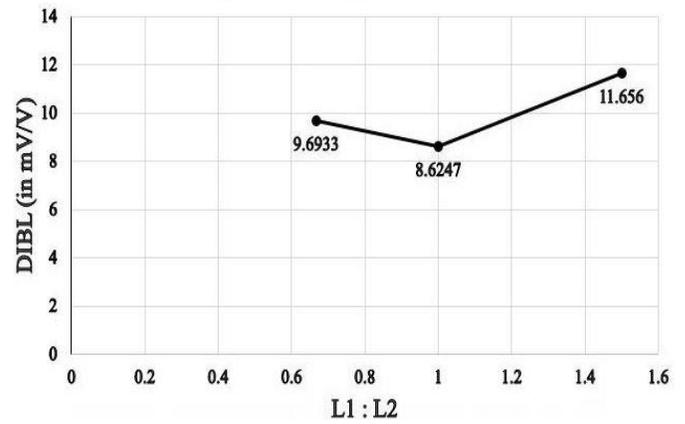


Fig. 7: DIBL graph for DMG FD SOI MOSFET for different L1:L2 using  $HfO_2$  as spacer material

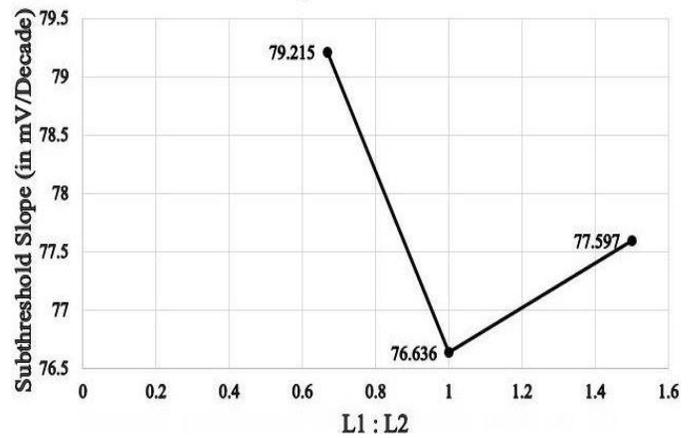


Fig. 8: Subthreshold Slope graph for DMG FD SOI MOSFET for different L1:L2 using  $HfO_2$  as spacer material

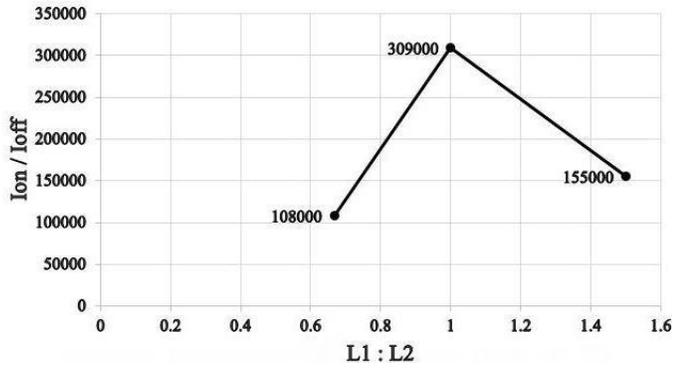


Fig. 9  $I_{on}/I_{off}$  graph for DMG FD SOI MOSFET for different L1:L2 using  $HfO_2$  as spacer material

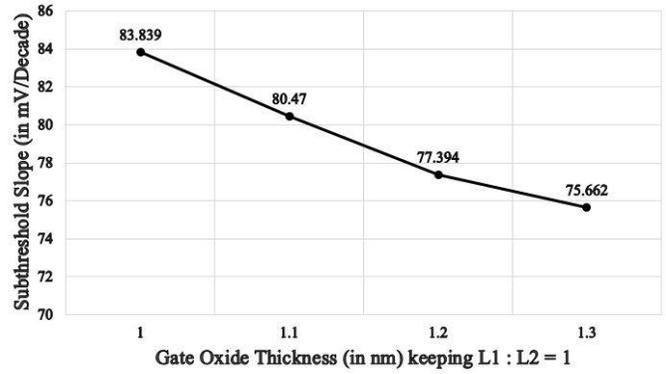


Fig. 12 Subthreshold Slope graph for DMG FD SOI MOSFET for different gate oxide thickness using  $Si_3N_4$  as spacer material

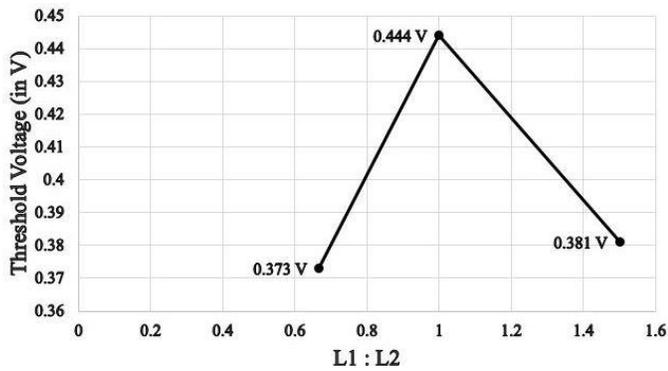


Fig. 10 Threshold voltage graph for DMG FD SOI MOSFET for different L1:L2 using  $HfO_2$  as spacer material

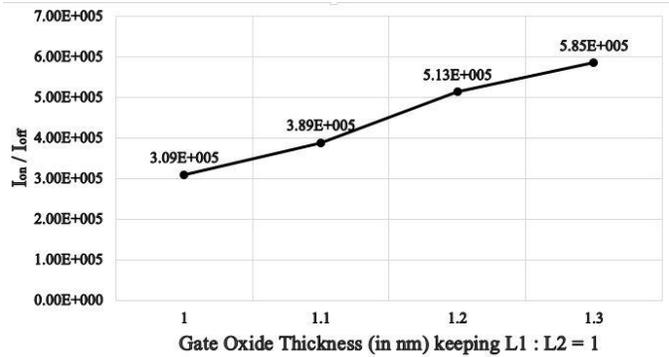


Fig. 13  $I_{on}/I_{off}$  graph for DMG FD SOI MOSFET for different gate oxide thickness using  $Si_3N_4$  as spacer material

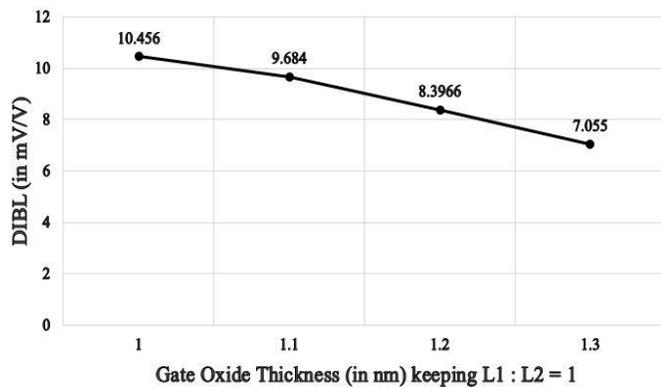


Fig. 11 DIBL graph for DMG FD SOI MOSFET for different gate oxide thickness using  $Si_3N_4$  as spacer material

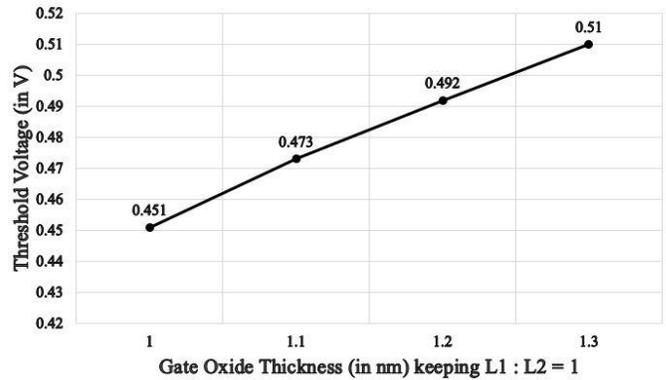


Fig. 14 Threshold voltage graph for DMG FD SOI MOSFET for different gate oxide thickness using  $Si_3N_4$  as spacer material

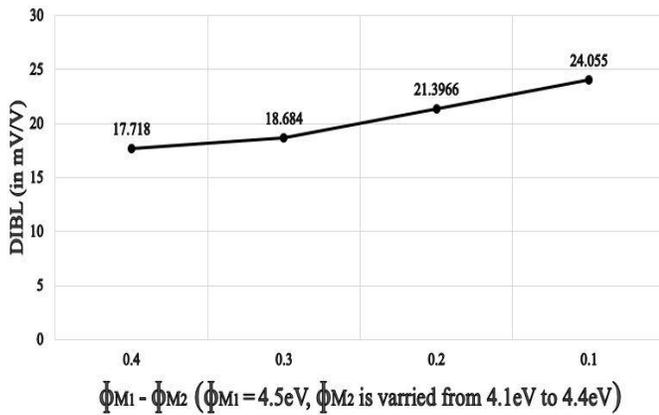


Fig. 15 DIBL graph for DMG FD SOI MOSFET for different work function difference between two gate metals using SiO<sub>2</sub> as spacer material

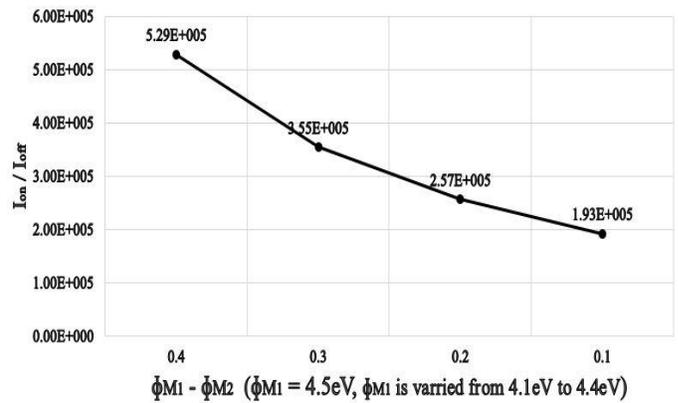


Fig. 18 Ion/Ioff graph for DMG FD SOI MOSFET for different work function difference between two gate metals using SiO<sub>2</sub> as spacer material

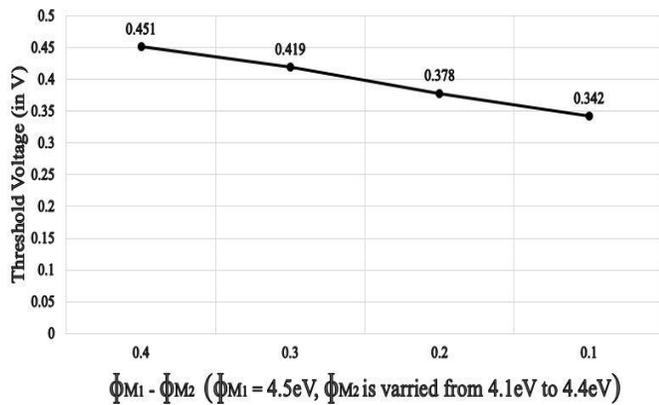


Fig. 16 Threshold voltage graph for DMG FD SOI MOSFET for different work function difference between two gate metals using SiO<sub>2</sub> as spacer material

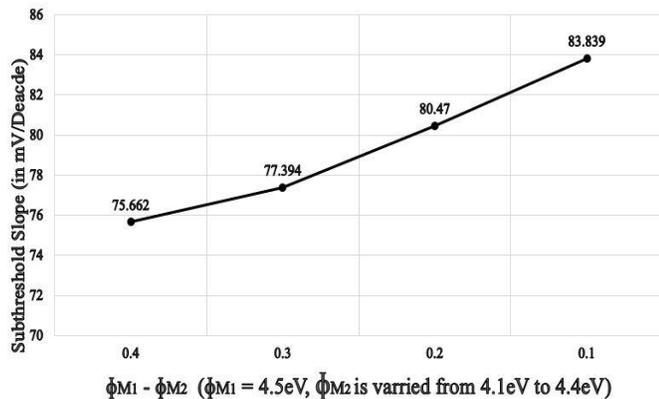


Fig. 17 Subthreshold Slope graph for DMG FD SOI MOSFET for different work function difference between two gate metals using SiO<sub>2</sub> as spacer material

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