Interleaved Sepic Converters for AC-DC Front-End Converter Application

Dr. D. Anto Sahaya Dhas¹, Dr. G. Justin Sunil Dhas², and Anand K³

Abstract—In ac/dc power factor correction (PFC) applications, where a wide range dc link voltage is required, boost derived topologies are no longer the most suitable circuit topologies for universal grids. In this paper an interleaved SEPIC converter, capable of providing a wide range dc link voltage is investigated. The interleaved converter is able to process more power with reduced circuit ripples and harmonics distortion, and current stresses. Additionally, because the coupled inductors share a common magnetic core, the count of magnetic devices is kept the same as the single-phase topology. Moreover, using coupled inductors effectively solves the current sharing problems caused by the duty cycle mismatch. The phase of the gate signals among different phases can be artificially shifted by a certain degree which would contribute to reduce the circuit harmonics as well as the current ripples.

Keywords—Converter, SEPIC, filter, duty cycle, boost, buck

I. INTRODUCTION

Many of the industrial as well as residential applications require dc-dc converters and these converters should be capable of providing higher power density, high conversion efficiency and low electromagnetic interference (EMI) and low noise level. In solar applications and wind turbines the generated voltage and current will exhibit a non-linear v-i characteristics and the maximum power point will vary with solar insolation in case of p-v cells and wind speed in case of wind turbines. So the intermediate DC-DC converter should be capable of adjusting the voltage and current levels and vary the load so as to extract maximum power from the load [1]. Also many of the electrical equipment will require front end ac-de converters which will consists of a diode bridge rectifier. This rectifier action will cause a non-linear current to be drawn from the ac line which causes wave form distortion, harmonic generation and related problems. So a dc-de converter with power factor correction should be employed between the rectifier and reservoir capacitor.

In conventional approaches, the basic converters like buck, boost, buck-boost and derived topologies like Luo, Cuk and SEPIC are commonly used[2],[3]. Among these SEPIC topology is more preferred because its capability to provide buck and boost operation without polarity reversal, reduction in input and output current ripple, voltage ripple and lower switching stress but with a penalty of higher number of components.

In this paper, an analysis of an interleaved sepic converter was carried out. An interleaved converter with two sepic converters connected in parallel was considered for this work. The performance of the conventional sepic and interleaved sepic were compared by means of simulation. Simulation of the system was carried out using MATLAB/Simulink.

II. ADVANCING POWER RATING OF PFC CONVERTER

The power level of a power electronic converter is limited due to several factors. Increasing current increases stresses on switching devices, diode reverse recovery current and parasitic resonance currents become greater than the main switch can handle, and the size of the boost inductor should be increased to avoid saturation and overheating problems. The component stresses can be reduced by controlling the turn off rate of the boost diode current by implementing passive or active snubber [4] circuits and the power level can be slightly advanced, but in order to advance the power level significantly the methods including device paralleling, module paralleling, power stage paralleling, and interleaving are widely utilized.

A. Interleaving

Interleaving of DC-DC converters is a well-established concept. It is widely used in power supplies and power factor correction circuits. In interleaved operation of dc converters also known as multiphase operation, several identical converters all switching at the same frequency are operated in parallel but with a uniform phase shift between them. This causes the ripple at the input and the output terminals of the converter to have a frequency that is a multiple of the switching frequency of each individual converter and the number of interleaving branches. Mathematically there is no limit for the number of interleaved power branches. But, in practice as the phase number increases, the system complexity increases and control and maintenance becomes difficult. The main advantage of interleaving is the reduction of input current and output voltage ripples with smaller magnetic material volume than other methods. The input EMI filter size and output capacitor size are reduced in proportion with the ripple reduction. The disadvantage of the interleaving method is increase in the gate driving logic complexity, but necessarily the size and cost of the gate drive. Logic signals to all the gates are equally phase shifted by the amount defined as

\[ PS = k \frac{2\pi}{N} \]

N denotes the number of interleaved branches and k denotes the order of discrete interleaved branches (k = 1, 2, ..., N).[5]
According to the operating requirements, duty cycle of the converter should be varied. Therefore the degree of ripple cancellation is also varying parameter. The most optimum cancellation of ripple is a function of the duty cycle of the converter and the number of phases [6]. A method of measuring the variation of the ripple cancellation as duty cycle is varied is by using the factor $F_c$ as shown in figure[7],[8]. The factor $F_c$ is a ratio of the ripple magnitude of the interleaved converter to the magnitude of the ripple in one individual phase or converter. From the fig.1 it can be seen that, maximum ripple cancellation is obtained for a duty ratio of 0.5 and the percentage of ripple content increases when duty ratio moves towards zero and one.

**Fig.1. Ripple cancellation Factor $F_c$ Vs duty cycle**

III. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Single-ended primary inductor converter (SEPIC) is a derived dc-dc converter whose output voltage can be more, less, or equal to the input voltage depending up on the duty ratio. That is the sepic can provide buck boost operation without polarity reversal.

Interleaving technology has been used in the proposed SEPIC in order to further reduce the filter size, and gain higher efficiency. In the interleaved configuration, we parallel n SEPIC cells, and artificially shift the phase of the gate signals by $2\pi/n$, some ripple can be totally cancelled due to the phase shift and the RMS current of output capacitor is reduced. Therefore, the size of output capacitor and EMI filter can be greatly reduced.

**A. Modes of Operation**

The operation of interleaved sepic is similar to the conventional sepic. In boost mode of operation since duty ratio is greater than 0.5, firing pulses of both converter will overlap each other. So at-least one switch will be on for entire operating cycle. But in buck mode, there will be no overlapping between the firing pulses. So one switch will remain off during some time of the operating cycle.

For the converter, the values of all capacitors are taken to be sufficiently large so that they will block the direct current. Hence the average value of current flowing through them is zero. The inductors L3 and L4 are only source of load current. So average current through these inductors will be same as load current.

A SEPIC is said to be in continuous-conduction mode if the current through the inductor L1 and L2 never go down to zero. During a SEPIC's steady-state operation, the average voltage across capacitor C1 and C2 is equal to the input voltage (Vin). Because capacitors C1, C2 blocks direct current, the average current across it is zero, making inductor L1 and L2 the only source of load current. Hence the average current through inductor L2 is the same as the average load current and hence independent of the input voltage.

The operation of boost converter in boost mode is explained below.

**Mode 1**

![Mode 1 operation](http://dx.doi.org/10.15242/IIE.E0816013)

In mode 1, switch S1 is on and S2 is off. Capacitors C1 and C2 are charged to input voltage with left plate positive. Inductor L3 will be charging and capacitor C2 will be discharging through S2 and L4. This makes the diode D2 to be reverse biased. Since S1 is off, D1 will be forward biased and inductor L1 and L2 will be discharging through the load.

**Mode 2**

![Mode 2 operation](http://dx.doi.org/10.15242/IIE.E0816013)
In this mode, both switches are turned on, hence all inductors will be charging.

**Mode 3**

S1 is turned on and S2 is turned off. So current in L1 and L2 will be increasing and that of L3 and L4 will be decreasing.

**Mode 4**

Here both switches are turned off. Hence all inductors will be discharging.

Circuit wave form for boost operation is shown in figure. 7. For boost operation, inductor charging time will be greater than discharging time. Similarly, the wave form for buck operation is given in figure 8. For buck mode, inductor charging time will be less than discharging time.

IV. DESIGN EQUATION OF PFC SEPI Converter

The operation of the SEPIC depends upon the constant current in the intermediate ripple-filter inductor (L3 and L4). The selection of Boost inductor (L1 and L2) and capacitors C1, C2, and Co is based on allowable ripple current and voltage and is given by following equations.

Output voltage \( V_O = D \cdot V_{in}/(1-D) \)

Boost inductor \( L_1, L_2 = D \cdot V_{in}/[f_s \cdot (\Delta I_L_i)] \)

Intermediate capacitor \( C_1, C_2 = D \cdot V_{dc}/[(R \cdot f_\text{s}) \cdot (\Delta V_C_i)] \)

Output filter inductor \( L_3, L_4 = (1-D) \cdot V_{dc}/[f_s \cdot (\Delta I_L_o)] \)

Output filter capacitor \( C_0 = I_{av} / (2 \cdot \omega \cdot \Delta V_{dc}) \)

The symbols used are \( f_s \) for switching frequency; \( V_{in} \) for average input voltage of SEPIC converter; \( D \) for Duty cycle; \( \Delta I_L_i \) for Peak to peak ripple current \( I_{Li} \); \( \Delta I_L_o \) for Peak to peak ripple current \( I_{Lo} \); \( \omega \) and \( \Delta \) for filter inductor and Boost inductor respectively; \( C_0 \) and \( C_i \) for filter capacitor and Boost capacitor respectively; \( I_{av} \) for average DC output current;

**TABLE I**

<table>
<thead>
<tr>
<th>Calculated Parameters</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input voltage</strong></td>
<td>( V_{in} = 20-30 \text{V} )</td>
</tr>
<tr>
<td><strong>Output voltage</strong></td>
<td>( V_O = 24 \text{V} )</td>
</tr>
<tr>
<td><strong>Output power</strong></td>
<td>( P_O = 120 \text{W} )</td>
</tr>
<tr>
<td><strong>Switching frequency</strong></td>
<td>( f_s = 110 \text{KHz} )</td>
</tr>
<tr>
<td><strong>Inductors</strong></td>
<td>( L_1=L_2=L_3=L_4=110 \mu \text{H} )</td>
</tr>
<tr>
<td><strong>Capacitors</strong></td>
<td>( C_{in}=820 \mu \text{F} ; C_0=470 \mu \text{F} ; C_1 = 2.2 \mu \text{F} );</td>
</tr>
</tbody>
</table>
V. SIMULATION AND RESULTS

As per the design equations, a two phase interleaved SEPIC converter with coupled inductors is simulated in MATLAB SIMULINK.

Fig. 9 Simulink model of proposed converter
Here PWM technique is used for generation of gating signals. A triangular wave of amplitude one is compared with duty ratio to obtain gating signal of S1. Switch S2 should be fired with a phase shift of 180. So peak of triangular wave minus duty ratio is compared with triangular wave to obtain duty ratio of switch S2.

The benefit of using the interleaved architecture comes from its reduced current ripple and reduced THD. This is mainly because the inductor current ripples in each individual SEPIC branch cancel with each other. The maximum ripple cancellation is obtained for duty ratios of 0.5 since current waveform in two phases are identical but exactly phase shifted by 180. Due to the reduced current ripple, the harmonics components are also significantly reduced. Therefore, the proposed circuit is featured with reduced THD.

Interleaving effect also brings the benefit of smaller output voltage ripple at the switching frequency. It should be noted that the output voltage ripple is equal to the stored charge variation on the output capacitor divided by its capacitance. For single phase SEPIC converter in continuous conduction mode, the output voltage ripple is $d\frac{TsIo}{Co}$. For interleaving SEPIC converter, in CCM operation, the voltage ripple can be derived as $(d-0.5)\frac{TsIo}{Co}$, which is much smaller than the voltage ripple of single phase converter. This reduced output voltage ripple represents reduced RMS current on the output capacitor. This can be translated into reduced conduction losses, reduced heat dissipation, and better system reliability.

Interleaving and paralleling power converters can increase the efficiency of the power converter; as long as, the inductor ripple currents are kept within reason. The semiconductor switching losses will remain roughly the same. The conduction losses should be reduced with each additional phase. However, if the inductor currents have excessive inductor ripple the higher RMS currents will cause greater conduction losses driving down efficiency. Also at lower power levels where the switching losses dominate interleaving will not show a drastic improvement in efficiency.

In a two-phase converter, there are two output stages that are driven 180 degrees out of phase. By splitting the current into two power paths, conduction losses can be reduced, increasing overall efficiency compared to a single phase converter. Because the two phases are combined at the output capacitor, effective ripple frequency is doubled, making ripple voltage reduction much easier. Likewise, power pulses drawn
from the input capacitor are staggered, reducing ripple current requirements.

An interleaved topology, however, improves converter performance at the cost of additional inductors, power switching devices, and output rectifiers. Since the inductor is the largest and heaviest component in a power boost converter, the use of a coupled inductor, where a core is shared by multiple converters instead of using multiple discrete inductors, offers a potential approach to reducing parts count, volume, and weight. Coupled inductor topologies can also provide additional advantages such as reduced core and winding loss as well as improved input and inductor current ripple characteristics. Properly implemented, the coupled inductor can also yield a decrease in electromagnetic emission, an increase in efficiency, and improved transient response. Inductor flux coupling can be realized using either direct or indirect winding configurations and is a primary design consideration for the interleaved topology.

### VI. Conclusion

In this paper, an interleaved and coupled SEPIC converter is proposed for front end power factor correction. To evaluate some of the benefits of interleaving a 120W two phase interleaved SEPIC was simulated in MATLAB. This design could easily be upgraded to higher power by the proper selection of power components. Also, since the selection of output voltage and input voltage are at the designer’s discretion, the basic design could be adapted to many battery-powered applications.

Interleaving PFC pre-regulators has many benefits. It can reduce EMI and boost inductor magnetic volume. The amount of reduction varies and depends on the design requirements and design tradeoffs. The designer may choose to reduce either the boost inductor magnetic volume or cut back the switching frequency to reduce the size of the EMI filter. In some cases just adding an additional phase will reduce the size of the EMI filter. Interleaving also reduces the RMS current in the boost capacitor greatly reducing electrical over stress on the capacitor. However, the complexity and cost of the design will increase with each additional phase.

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