Abstract—Artificial neuron is a circuit that aggregates all synaptic inputs, applies it to an activation function and threshold to the result. Activation functions for hidden units are needed to introduce nonlinearity into neural network. The mathematical and bounding properties of activation functions in the realm of multi layer perceptrons are taken into consideration while designing CMOS activation function. Here, our work is to implement CMOS Sigmoid activation function. Their functional results are verified for use in voltage mode circuits for design of pulsed neural network using CADENCE SPECTRE 6.6.1

Keywords—Neural Network, Activation Function, CMOS operation.

I. INTRODUCTION

To implement neural network (NN) as analog circuitry, CMOS techniques can be used. MOSFETs as switches can pass either digital or analog signals coded as current or voltage. Without nonlinearity, hidden units would not make nets more powerful than just plain perceptrons [1]. Neuron output depends on level of activation. Activation function models internal aggregated cell potential.

Generally for any jth artificial neuron, if we consider an input signal $\delta_j$ having weighted pathways $W_{ij}$ with internal activation $X_j$ and internal threshold $\theta_j$. The Internal activation can be given by,

$$X_j = \sum W_{ij} \delta_i + \theta_j$$  \hspace{1cm} (1)

In neural networks, pulse bursts are formed by some neurons with longer or defined intervals [6]. Synaptic activity, cell morphology and electrical properties of membrane in the dendrite of neuron establish the behavior of the pulse [3,5]. For pulse-based neural circuits, there are various ways of modulating pulses. The following design uses PWM technique [8, 9]. Section 2 discusses general sigmoid function along with it’s analog implementation and discusses it’s results using CADENCE SPECTRE 6.6.1 in 180nm technology. Section 3 concludes on the development and use of the designed activation function.

II. CMOS Sigmoid Circuit

A. Sigmoid and tanh(nx) Functions

Sigmoid function is a smooth version of step function. It is zero for low input. At some point, it starts rising rapidly and at even higher levels of input, it saturates. Naturally, such a property can be noticed biologically, where the firing rates of neurons are limited by certain conditions.

A simple comparison of Sigmoid and Hyperbolic Tangent functions as inbuilt functions in MATLAB is observed in Fig.2.

Fig. 2: Sigmoid and tanh(nx) functions

![Fig. 2: Sigmoid and tanh(nx) functions](image-url)
B. Analog Implementation of Sigmoid Function

In PWM operations, design criteria is better set in analog as PWM circuits are localized. The hand calculations are done with help of process and model parameters as described by BSIM3V3 manual and gpdk180 process files used in Cadence Virtuoso 6.1.6[2, 7]. Using material and device parameters, CMOS design to meet the specifications has been designed where \( k' \) is transconductance parameter, \( W \) is the channel width, \( L \) is the channel length, \( C_{ox} \) is the compensation capacitor, \( SR \) is slew rate, \( \mu_0 \) is the mobility factor, \( C_{ox} \) is the oxide capacitance.

\[
\text{Aspect ratio } S = \frac{W}{L}
\]

Chosen device length \( L = 1 \mu m \)

\[
\beta = k' \frac{W}{L} \quad \mu_0 C_{ox} \frac{W}{L} \quad (A/V^2)
\]
In Fig.1, For design of Voltage mode Sigmoid circuit, Vin is the input voltage, V_{\text{dc}}=abc is the controlling voltage used for parametric analysis and V_{\text{out}} is the output voltage. The power supply is kept at ±1.8V. The value of L=1µm and gpdk180 process is used to calculate values of aspect ratio.

**TABLE I: Aspect Ratios of the transistors**

<table>
<thead>
<tr>
<th>S=W/L</th>
<th>Calculated Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_1-S_6</td>
<td>3</td>
</tr>
<tr>
<td>S_7-S_8</td>
<td>2</td>
</tr>
<tr>
<td>S_9-S_10</td>
<td>1</td>
</tr>
<tr>
<td>S_{11}-S_{19}</td>
<td>3</td>
</tr>
</tbody>
</table>

V_{\text{out}} is the output and the DC analysis for V_{\text{in}} vs V_{\text{out}} shows the exponential curve as observed in output Fig.3. The result in Eq.3 is obtained.

$$V_{\text{out}} = \frac{1.8}{1 + e^{-4(V_{\text{in}}-0.9)}}$$  \hspace{1cm} (3)

This circuit can replace the working of Eq.1 while designing the entire Analog pulsed neural network using 180nm process technology in CADENCE SPECTRE 6.1.6.

**III. Conclusion**

A voltage mode CMOS based pulsed neural network using PWM technique includes a synapse multiplier, a voltage to pulse converter circuit and also needs an activation function unit. For that purpose, a Sigmoid function using CMOS is designed for activation function unit. Its working can be tested for training analog neural networks and implemented in neural chips. They have wide use in communication systems and few hearing aid designs.

**REFERENCES**


