A New Clustering Based Routing Algorithm for NoC

Abdelmalek Bouguettaya, Mohamed Taher Kimour, and Salah Toumi

***Abstract*--** With the increasing number of the integrated cores on a single chip, research into Network on Chip (NoC) becomes important. NoC has been proposed as a solution to replace the classic interconnections of Systems on Chip (SoCs) design. Topology and routing algorithm are important keys of the NoC design. In this paper, we propose a new fault-tolerant routing algorithm for Networks on Chip (NoCs). The proposed algorithm is based on a combination between a dynamic routing algorithm and a communication load clustering technique in a 2D mesh topology.

***Keywords* –** Networks on chip, Dynamic routing algorithm, Fault tolerance, Clustering, Mesh topology.

I. Introduction

BY the end of the decade, according to the International Technology Roadmap for Semiconductors [1], SoCs will grow to 4 billion transistors running at 10 GHz and operating below one volt [2].Typically, in these systems, a several complex heterogeneous components can be integrated such as programmable processors, memories, input–output interfaces, custom hardware, peripherals, external interface IP (intellectual property) blocks that need to communicate with each other and an on-chip communication architecture that serves as the interconnection fabric for communication between these components. These elements serve to increase performance and to reduce cost and improve energy efficiency [2, 3].

Several architectures based on a bus communication have been proposed since 1990 to handle the communication needs of emerging SoC designs [4].While integration increases the bus structure reach its limits in term of performance and it does not meet the needs of the new technology. Bus starts to be narrow and in the worst case it begins to block traffic. It will be less used in 5 or 10 years.

The NoC is a new paradigm for System on Chip design [5]. This technology is come to replace the classic buses interconnection to interconnect the IP modules in SoCs.

Nowadays, Networks on Chip are considered as a scalable solution for on chip communication. In the recent years, Network on Chip has emerged as a growing and important research field.

Abdelmalek Bouguettaya, Salah Toumi, LERICA Laboratory, Department of electronic, email: amalek.bouguetaya@univ-annaba.org, salah.toumi@univ-annaba.org

Mohamed Taher Kimour LASE Laboratory, Department of computer science University of Badji Mokhtar-Annaba Po. Box 12, Annaba, Algeria, email: 2kimour@yahoo.com.

The most important aspects that distinguish the various NoC architectures are topology and routing algorithm. After determining the network topology, the routing algorithm is the responsible of deciding the path a message or a packet will take through the network to reach its destination.

Our approach is based on a combination between a clustering technique and a dynamic routing algorithm in a 2D mesh topology. We show that such the proposed approach enhances the performance of the routing algorithm and provide better fault-tolerance value.

The next section describes the Network on Chip technology (NoC) and its characteristics. In section 3, we present our approach. And finally, we conclude this paper and present the future works.

II. Network on Chip architecture

The Network on Chip is a new paradigm comes to replace the classic interconnections (Tab.1) as point to point, crossbar, bus, etc…2D mesh NoC architecture is the most used topology due to its regularity, simplicity for routing and easy integration in FPGA circuit.All the links have the same length, thus exhibiting the same latency.

TABLE I
THE ADVANTAGES PROVIDED BY NoCs.

problematic	Solution provided by the on-chip networks
Propagation delays	Minimal impact because the global interconnections are divided into shorter paths with the possibility of pipelining.
Clock distribution	Modular architecture and packets transport mode: adapted as well as the synchronous approaches than multi-synchronous or asynchronous approaches.
Bandwidth	Generally high as several transport paths can be used in parallel.
Scalability/Flexibility	Regular architectures easily expandable depending on the number of IP without major degradation of temporal and electrical performances.

Network on Chip is composed of three main building blocks (Fig.1). The first one is the link that allows connecting the nodes and transferring data between them and plays an important role in the performance of NoC architecture. The second block is the router; its main role is to route data from a source to a destination. The last building block is the network interface (NI). This block is composed of two parts: Network Interface (NI) and Network Adapter (NA). The first part allows to physically separating the calculation function to the communication function and allows the reuse of both, core and communication infrastructure independent of each other [6]. The second part realizes the adaptation of communication protocols between the resource and the router.

The NI is divided into two parts: a front end and a back end. This part is usually implemented as a socket – OCP [7], AXI [8], etc. The second part (back end) manages the network protocol (assembles and disassembles the packet, reorders buffers, etc.) (Fig.2).

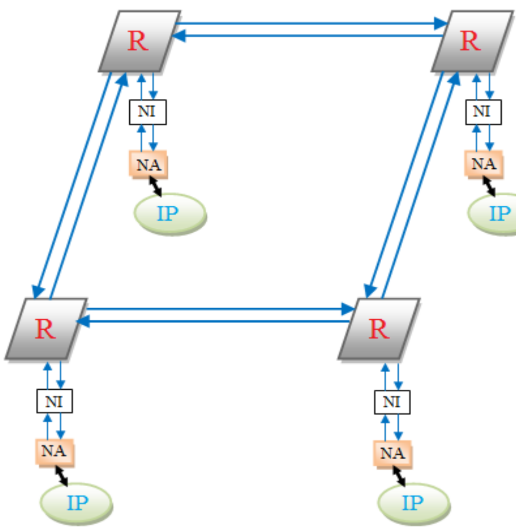

Fig. 1 the building blocks of NoC.

Recently, network-on-chip (NoC) research has focused on the various aspects of on-chip networks, including topology [9, 10], routing algorithms [11], flow control techniques [12], and router architecture [13, 14].

A. topology

A key point on the NoC performance is the interconnect topology. It is represented by a graph G (N, C) where N is the set of routers and C is the set of communication channels. The routers can be connected in direct or indirect topologies. NoC can be organized as different topologies, which determines the physical layout and connections between nodes and channels in the network [15]. There are many topologies used for NoCs, whether direct or indirect, regular or irregular. Evidently, the list of topologies that follows is not exhaustive but represents those most often used in NoCs, including mesh, torus, 3D mesh… (Fig.3). Due to its simplicity and its prevalence in several implementations we have chosen the mesh topology for our design.

For comparing topologies there are many metrics. The router degree of a topology refers to the number of links at each node. When all routers have the same degree, a topology is considered as regular, else it is considered as irregular. The second metric is the number of links traversed by a message from the source to the destination or called diameter. The third one is the maximum channel load which means the maximum number of bits that can be injected by every node into the network per second (bps) before it saturates [16].We mention also the path diversity.

The literature NoCs widely uses regular topologies. The standard topology is the 2D mesh one. It is adapted to the 2D integrated circuit technology and it is scalable. It allows the use of simple routing strategies and therefore inexpensive.

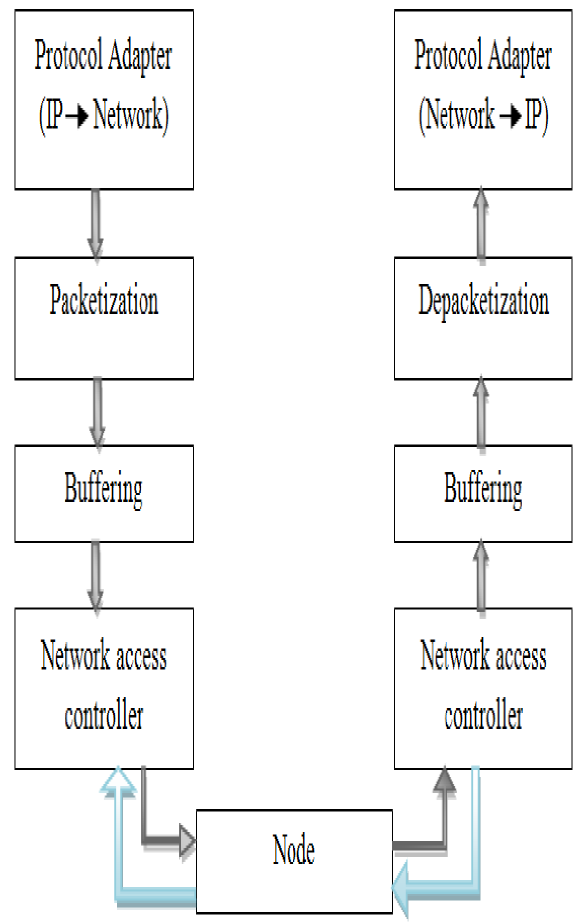

Fig. 2 Network Interface architecture.

B. routing

The routing algorithm is the next step after determining the network topology. The routing algorithm is the responsible of deciding which path has the message to follow to be effectively routed from its source to its destination. The purpose of the routing algorithm is to distribute traffic in the same way between the paths provided by the network topology, thus improving network latency and throughput.

Routing algorithms can be classified into three categories: deterministic, oblivious and adaptive or dynamic routing.

The deterministic one, to transfer data between a source and a destination pair, it takes always the same path. XY routing is one common used deterministic routing algorithm. In XY routing algorithm, the packet is always first routed in the (X direction), until it reaches the network node, which has the same X coordinate of the destination node. Then, the packet is routed in the (Y direction), until it reaches the destination node. The advantage of deterministic routing is his ability to avoid the deadlock problem.

http://dx.doi.org/10.15242/IIE.E0114006

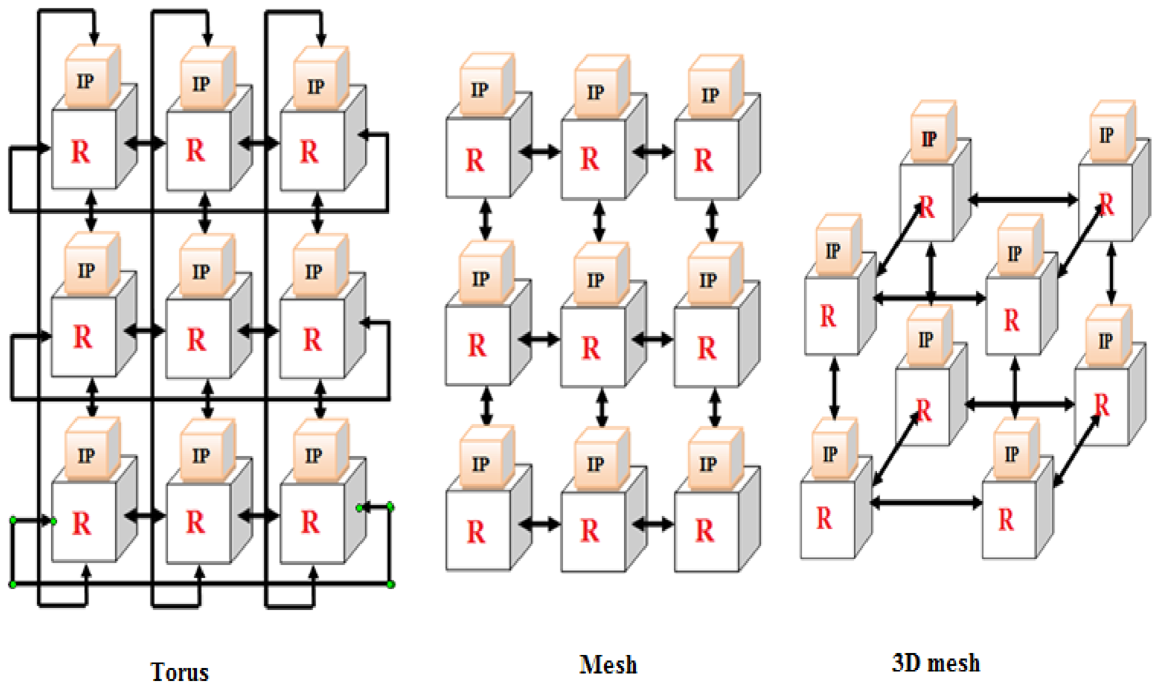

Fig. 3 Network on chip topologies.

The oblivious routing, routing paths are chosen without regard to the state of the network. By not using information about the state of the network, these routing algorithms can be kept simple. It is simple to implement and simple to analyze. The deterministic routing algorithm is a subset of oblivious routing.

The adaptive routing, the path taken by a message is not known a priori, but is determined as it propagates through the network.At each node through the routing function selects an output port based on a number of criteria. These criteria are mainly related to the network congestion and failure. The main idea behind this concept is to avoid/bypass network areas already heavily loaded.

C. Router Design

The router design plays an important role to decide the performance of NoC systems. The structure of routers in a NoC depends on the network topology. A 2 D mesh topology router is composed of: buffers, crossbar, routing and arbiter units organized as in figure 4. Generally, the router is consists of five bidirectional ports (North, South, East, West and Local), each input port have a FIFO buffer connected to the crossbar and the routing and arbiter units.

The buffers are for storing the packets transmitted in the network. The role of crossbar is to connect input ports to output ports. Routing and arbiter units which ensures the switching function and manages conflict situations.

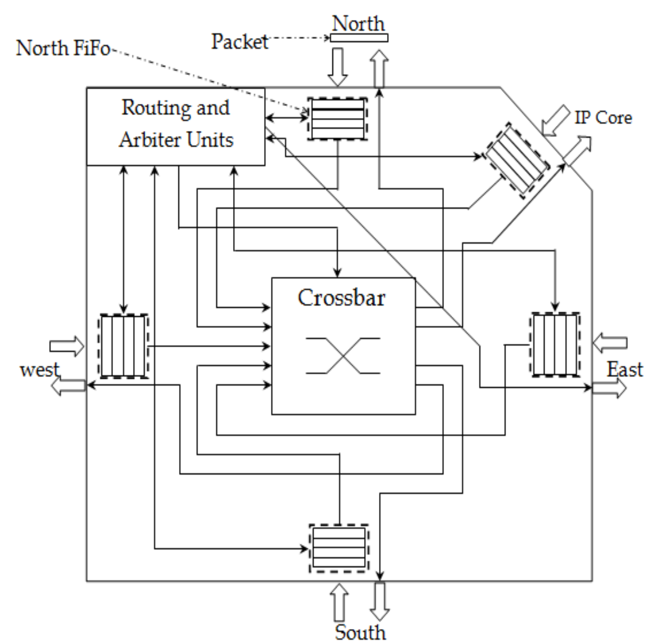

Fig. 4 Router architecture.

III. Presentation Of Our Routing Approach

In this section we will define our routing approach. It is based on the clustering of the nodes in groups (Fig.5). We partition the network into many clusters. Every cluster has a cluster header who has all the information about its members and the network state.

Clustering is a technique to partition nodes into groups according to certain property. Our clustering objective is to give an improvement to the link state routing to avoid the fail links and/or routers. In other words, we aim to make the search more efficient, while not limiting the search space.

Within the cluster, the goal of link state routing is for each peer to have an identical picture of the state of the entire cluster. Link state protocols require each router to know whether a link is up or down and which cost it has, and then calculate the total cost to reach a destination in the cluster.

Our clustering process aims at creating groups of nodes which resides in the same region and such that the sums of communication load should be smaller than a certain threshold.

The routing does into two levels in this approach (inter cluster and intra clusters).

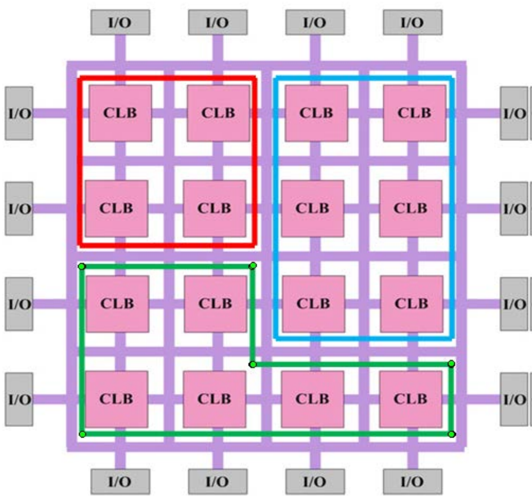

Fig. 5 Clustering of nodes.

A. Clustering algorithm

We can find many definitions of clustering technique in the literature. The simplest definition is to grouping similar nodes into the same cluster. The clustering is done according to certain rules as: the distance between each peer of nodes, the implemented application, the synchronization, etc… In our case we use the density of communication load between every point to point peer of nodes. We select a cluster header for each cluster. It contains additional information about the other cluster headers. There are many clustering techniques based on several criteria [17, 18].

In this section we present the steps of our density communication load based clustering technique. Firstly, the calculation of the communication load between every two nodes is done off line. To grouping nodes in a cluster, we generate a communication load graph.

Clustering in networks is an effective way to structure the network. Its purpose is to identify a subset of nodes in the network and assign a leader (cluster-head). Below we will mention some selection criteria of the cluster head.

- Without metric: includes algorithms that declare the cluster-headers without using any selection metric.
- Neighbor density: it’s a choice based on the number of neighbors.
- Arbitrary metric: in this class, we find algorithms that use random values or the identifying nodes.
- Metric related to the topology: in this class we group all algorithms that use a metric outcome of the network topology.

In our case, we choose the node that has the smallest communication load in a cluster as the cluster header to reduce its work to avoid breakdowns of the node. In the clustering technique, the cluster head becomes a bottleneck. As a solution of this problem, we choose the node that has the smallest communication load as a cluster header to reduce the number of traffic that passes through it. So it will play the role of managing intra cluster communications. The designation of a successor of cluster head is need in case of failure or breakdown. The choice is done in the same previous way, by using the calculation of the communication load density. The choice of the successor is done in the same time with the selection of the real cluster head.

Thanks to the combination of nodes that have the highest density of communication between them in the same cluster. This clustering technique offers many advantages and ameliorations. Among its advantages and ameliorations we cite the following:

- Minimize energy consumption: low power consumption is offered. by reducing the overall routing area.
- Reduce the communication time between nodes: such clustering technique offers a better latency.
- Reduce the detection time and reporting failures in links and / or routers (not need to inform all network members about the fault).
- Robustness: by ensuring the performance and stability of a system in the face of environmental disturbances and model uncertainties.
- The routing is more efficient: the clustering technique offers a diversity of paths.
- Optimize the use of resources: more efficient use of resources is offered by using the clustering technique.

B. Detail routing

In the following, we give a brief description of the significant steps that are carried out by the link state algorithm in a cluster of routers. The communication between nodes in the same cluster is done according the following steps:

1. On start up, a router gathers information about its peers by sending a HELLO packet on each point-to-point link. Upon receiving this packet, a router replies to the sender with its unique identifier. A consolidated routing table (CRT) is set at the cluster header.
2. Within the cluster, a router needs to calculate the delay or cost of each of its neighbors by sending an ECHO packet which should return it immediately in order to observe the turn-around time.
3. We use the gathered information to build a packet containing all this data by the routers in the cluster. This packet is then broadcast to every router (in the cluster) that can answer to this protocol, a process known as flooding, which means that it sends the information to all of its neighbours which in turn send it to all of their neighbours and so on. Soon, all routers on the cluster have this information.
4. The neighbour information is flooded whenever there is a routing-significant change in the cluster.

5. As every router knows everything about the cluster by structuring the information from other routers, it can calculate the best path to any host on any destination cluster at any time by using Dijkstra's "Shortest Path First" algorithm.

The communication between the source node and the destination node done without passing by the cluster head.

C. Global routing

In this section, we define the way how nodes of different clusters can communicate between them using a combination between the clustering technique and the link state routing algorithm. The related steps are as follows:

1. The cluster header of the sender cluster gathers information from the other clusters headers in the network (also the destination cluster).

2. When a source node in cluster Cs wants to send a packet to a destination node in another cluster Cd, it submits this packet to the header in Cs using the above-mentioned steps (at cluster level).

3. The cluster header in Cs selects the path according to appropriate parameters and sends the packet to the cluster head Cd.

In figure 6, we illustrate the way to send a packet from a source node to a destination node involving deferent clusters. Indeed, the packet can take different ways to reach its destination. The source node sends the packet to the cluster head and this last one chooses between the possible ways to reach the destination node. Then, the cluster head sends the packet after collecting information about the other cluster heads of the other clusters and sends the packet in the way to avoid the link fail. The cluster head sends the packet in the best way to achieve his destination.

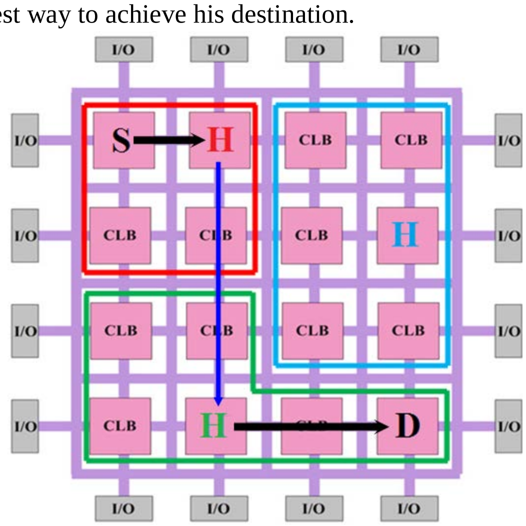

Fig. 6 Communication in the global level.

IV. Conclusion

In NoCs, the routing algorithm affects the performance of such systems. Performance requirements are small latency, guaranteed throughput, path diversity, sufficient transfer capacity and low power consumption. In this paper we have presented an adapted routing algorithm which can take full advantage of routing resources of various types. It is based on a combination between the link state algorithm and the clustering techniques. Our approach provides the minimization energy consumption, Reduce the communication time between nodes, reduce the detection time and reporting failures in links and / or routers (not need to inform all network members about the fault), optimizes the resources use and the routing is more efficient. We also identified the most relevant metric for evaluating the performance of clustering algorithms. As a future works, we plan to evaluate our approach using experiments.

References

[1] Semiconductor Industry Association. International Technology Roadmap for Semiconductors (ITRS), 2001. http://public.itrs.net.

[2] T. Kogel, R. Leupers and H. Meyr, "Integrated System-Level Modeling of Network-on-Chip enabled Multi-Processor Platforms," Springer Edition, 2006.

[3] H. Chang, L. Cooke, M. Hunt, G. Martin, A. McNelly and L. Todd, "Surviving the SOC Revolution - A Guide to Platform-Based Design," Kluwer Academic Publishers, 1999.

[4] S. Pasricha and N. Dutt, "On Chip Communication Architectures: System on Chip Interconnect," ELSEVIER Edition, 2008.

[5] L. Benini and G. Micheli, "Network on Chips: A new SoC Paradigm," IEEE Computer, 2001.

[6] T. Bjerregaard and S. Mahadevan, "A survey of research and practices of network-on-chip," ACM Computer Survey, 2006. http://dx.doi.org/10.1145/1132952.1132953

[7] OCPIP (2011) http://www.ocpip.org/. Accessed 25 May 2011.

[8] ARM (2011) AMBA advanced extensible interface (AXI) protocol specification, version 2.0.http://www.arm.com. Accessed 26 May 2011.

[9] J. Kim, J. Balfour, and W. J. Dally, "Flattened Butterfly for On-Chip Networks," In Annual IEEE/ACM International Symposium on Micro architecture (MICRO), 2007.

[10] B. Grot, J. Hestness, S. W. Keckler, and O. Mutlu, "Express cube topologies for on-chip interconnect," In International Symposium on High-Performance Computer Architecture(HPCA), 2009.

[11] D. Seo, A. Ali, W.-T. Lim, N. Rafique and M. Thottethodi, "Near-optimal worst-case throughput routing for two-dimensional mesh networks," In Proc. of the International Symposium on Computer Architecture (ISCA), 2005.

[12] A. Kumar, L.-S. Peh, P. Kundu, and N. K. Jha, "Express virtual channels: Towards the ideal interconnection fabric," In Proc. of the International Symposium on Computer Architecture (ISCA), 2007.

[13] H. Matsutani, M. Koibuchi, H. Amano, and T. Yoshinaga, "Prediction router: Yet another low latency on-chip router architecture," In International Symposium on High-Performance Computer Architecture (HPCA), 2009.

[14] P. Abad, V. Puente, J. A. Gregorio, and P. Prieto, "Rotary router: An efficient architecture for cmp interconnection networks," In Proc. of the International Symposium on Computer Architecture (ISCA), 2007.

[15] PP Pande, C Grecu, A Ivanov and R Saleh, "Performance evaluation and design trade-offs for network-on-chip interconnect architectures," IEEE Trans Comput., 2005. http://dx.doi.org/10.1109/TC.2005.134

[16] N. E. Jerger and L. S. Peh, "Network On chip," Morgan & Claypool Edition, 2009.

[17] D. Wei and H. A. Chan, "Clustering Ad Hoc Networks: Schemes and Classifications," Proceedings of the 3rd Annual IEEE Communications Society on Sensor and Ad Hoc Communications and Networks (SECON'06), 2006.

[18] R. Agerwal and M. Matwani, "Survey of Clustering Algorithms for MANET," International Journal on Computer Science and Engineering, 2009.