Hardware Verification of Forward Clarke Transform Based Algorithm Data Flow on FPGA for Green Technology

Muhazam Mustapha, Nik Ghazali Nik Daud, and Siti Nursyuhada Mahsahirun

***Abstract*—** This paper presents the implementation of Forward Clarke Transform (FCT) module on Field Programmable Logic Controller (FPGA) using Verilog hardware description language (HDL). FCT is mathematically represented in matrix form and used to convert a three-phase Permanent Magnet Synchronous Motor (PMSM) stator current into two-phase quadrature current. The input and output (I/O) interphase signals i.e. ia and ib, iα and iβ are all in 2's complement 16 bits. To address the complicated hardware based floating arithmetic, floating point calculations involved are handled as fixed-point. The module has also successfully computed the FCT calculation within four clock cycles both on simulation and real experiment Altera DE II FPGA.

***Keywords*—**Forward Clarke transform, space vector, reluctance motor control, hardware description language.

I. Introduction

A. Green Technology Connection

ONE of the considerations in ensuring an environmentally friendly technology is the efficiency of energy used in driving electric motors. Examples of areas where efficiency improvement can be made in electric motors driving are electrical braking, oscillation and overshooting reduction, field weakening control, motion profiling, etc. In many parts of these processes, multiphase system calculations are used. A common example for this is the calculation involving transformations between two phase system and three phase system.

This article is to publish the development process of a green technology compliant motor controller. The findings are part of the development that involved Forward Clarke Transform (FCT). The result in this part of the development would be utilized to build the 3 to 2-phase system converter that would later be used by other parts of a system of green technology motor controller.

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B. Mathematical Background

Clarke Transform is a mathematical transformation of three-phase coordinates into two-phase orthogonal time-varying coordinates system represented in matrix form. It was introduced in 1950 by Edith Clarke, a professor of electrical engineering from the University of Texas at Austin [10] [6]. Clarke's derivation involved space vector concept. It is also sometimes known as αβ, αβγ or dq0 transformations. In contrast to the complex representation in Clarke's derivation, real vectors representation is more convenient to be handled, where distinction between space and time phasor [11] is more evident. Equation (1.2) and Figure 1 express the simple derivation of the three vectors in a space by two axis system.

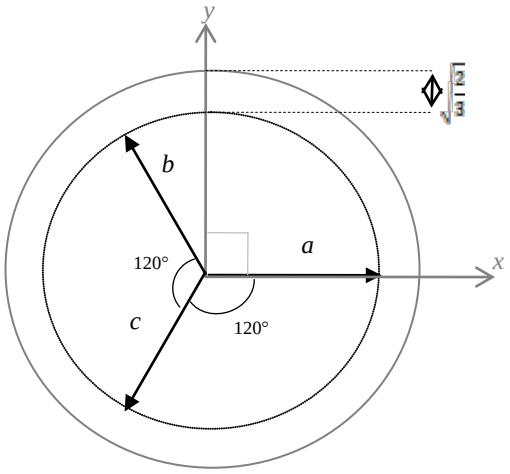

Fig. 1 Balanced three phase system

Equalizing coefficient to modify the actual locus represented by the inner circle to form the outer locus as indicated in Figure 1, i.e. $\sqrt{2/3}$, is applied to the equation to conserve power between the coordinate systems [5][12]. The $1/\sqrt{3}$ is obtained from Hermitian symmetrical components transformation while $\sqrt{2}$ coefficient is to produce the same instantaneous active power in the original coordinates and space vector frame in a symmetrical system. In the theory, factor $\sqrt{2/3}$ is used to achieve power-invariant transformation [8], however, as far as the module is concerned, the coefficient

2/3 can be used instead of $\sqrt{2/3}$. Equation (1.2) is the FCT equation used in this module.

From Figure 1,

$$\begin{bmatrix} x \\ y \end{bmatrix} = \mathbf{a} + \mathbf{b} + \mathbf{c}$$

$$= a\begin{bmatrix} 1 \\ 0 \end{bmatrix} + b\begin{bmatrix} -1/2 \\ \sqrt{3}/2 \end{bmatrix} + c\begin{bmatrix} -1/2 \\ -\sqrt{3}/2 \end{bmatrix}$$

$$\begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1.1)$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1.2)$$

In a balanced three phase power system, we know that,

$$i_a + i_b + i_c = i_a \angle 0° + i_b \angle 120° + i_c \angle -120°$$

$$= i_{peak}(1 - 0.5 + j0.866 - 0.5 - j0.866)$$

Thus,

$$i_a + i_b + i_c = 0 \quad (1.3)$$

From Equation (1.2),

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3}ia - \frac{1}{3}ib - \frac{1}{3}ic \\ \frac{1}{\sqrt{3}}ib - \frac{1}{\sqrt{3}}ic \end{bmatrix} \quad (1.4)$$

$$i_\alpha = \frac{2}{3}i_a - \frac{1}{3}i_b - \frac{1}{3}i_c$$

$$= \frac{2}{3}i_a + \frac{1}{3}i_a - \frac{1}{3}i_a - \frac{1}{3}i_b - \frac{1}{3}i_c$$

$$= i_a \quad (1.5)$$

and substituting $i_c = -i_a - i_b$,

$$i_\beta = \frac{1}{\sqrt{3}}i_b + \frac{1}{\sqrt{3}}i_c$$

$$= \frac{2i_b - i_a}{\sqrt{3}} \quad (1.6)$$

In basic Field Oriented Control (FOC) motor, Clarke's transform is utilized as reference to construct Park's transform frame. The pairing of Clarke's and Park's transforms constitutes collaboration to convert stationary reference plane to rotating reference plane [7]. It is also used as reference signal for the space vector modulation (SVM) of the three-phase inverter. The implementation of both Clarke's and Park's transform in FOC motor makes AC motor controllable as DC motor under steady state condition [7].

Mathematically describing motor requires a study of both rotor and stator electrical and magnetic elements. The interaction between rotor and stator magnetic flux (ϕ_r and ϕ_s) triggers mechanical movement. Stator induces rotating magnetic field (B_S) and it will agitate rotor's magnetic field (B_r). This will induce a mechanical force on the rotor to rotate to get back the right alignment against ϕ_s. In a reluctant machine such as permanent magnet synchronous motor (PMSM), rotor's flux is fixed relative to its physical structure. Hence, the implementation of controller for reluctant machines shall include the manipulation of stator current (I) value.

II. Algorithm Framework

The main approach used to complete this project was through a design methodology called data flow design [13] while the platform used was Altera DE II Board with Quartus II software IDE using Verilog [1]. With data flow design, it is possible to achieve the result in only 1 clock cycle while RTL (register transfer level) design may require more. However the trade-off is that the requirement for FPGA resources, which is 17 logic elements (based on Quartus II compilation report) in this case, is relatively high for a simple system like this. The reason for this is our utilization of Altera's built-in fast multiplier that uses a lot of logic elements.

Verilog handles signed number in 2's complement representation [9] which allows an easy conversion of multiplication by powers of 2 into signed shift: using >>> and <<< (instead of >> and <<). This concept can be seen in the module in Figure 3.

Most of the calculation would be to calculate iβ since iα is an obvious direct wiring from ia. The part of the iβ equation that involves division by √3 would be converted into multiplication by 1/√3 which is 0.57735026 in decimal. Converting this value into 16 bit binary fraction and shifting it to the left for 16 bits (to maintain integer calculation – i.e. fixed point calculation) will result in a hexadecimal value of 93CD hex. The use of 16 bit 2's complement format is to comply with the Micro Architecture Specification (MAS) [2] as provided to the team. At the end of the calculation, the final result will be right shifted for 16 bits, to compensate for the 16 bit left shift in 93CD hex, so that the correct result can be obtained.

The multiplication with 93CD hex would be using a fast scheme. There are many algorithms have been created to perform this including Booth algorithm invented by Andrew Donald Booth in 1951 [14]. In Altera Quartus II library, there is an embedded fast multiplier supporting signed number multiplication [4] [3] available. This is the one that has been used in this module.

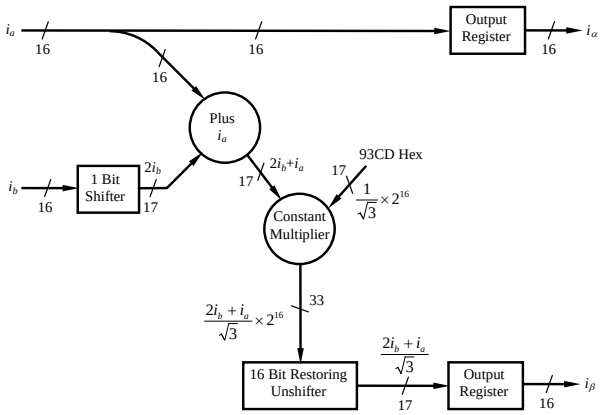

Fig. 2 Data flow design diagram

```
module FCT
(
input signed [16:0] ia, ib,
output signed [16:0] ialpha, ibetha
);

assign ialpha = ia;
assign ibetha = (((ib<<<1)+ia)*16'h93CD)>>>16;

endmodule
```

Fig. 3 The complete module

III. Hardware Implement, Result and Discussion

Both functional and timing analysis was done using waveform simulation by assuming the range of *ia* and *ib* is 0000 0000 0111 1111_2 (+12710) to 1111 1111 1000 0001_2 (−12710).

TABLE I
THE DESIRED INPUT AND OUTPUT MAPPING

θ (π rad)	i_a	i_b	ialpha	ibetha
0.0	0.0000	−109.9852	0.0000	−127.0000
0.1	39.2452	−124.2247	39.2452	−120.7842
0.2	74.6487	−126.3043	74.6487	−102.7452
0.3	102.7452	−116.0203	102.7452	−74.6487
0.4	120.7842	−94.3794	120.7842	−39.2452
0.5	127.0000	−63.5000	127.0000	0.0000
0.6	120.7842	−26.4048	120.7842	39.2452
0.7	102.7452	13.2751	102.7452	74.6487
0.8	74.6487	51.6556	74.6487	102.7452
0.9	39.2452	84.9796	39.2452	120.7842
1.0	0.0000	109.9852	0.0000	127.0000
1.1	−39.2452	124.2247	−39.2452	120.7842
1.2	−74.6487	126.3043	−74.6487	102.7452
1.3	−102.7452	116.0203	−102.7452	74.6487
1.4	−120.7842	94.3794	−120.7842	39.2452
1.5	−127.0000	63.5000	−127.0000	0.0000
1.6	−120.7842	26.4048	−120.7842	−39.2452
1.7	−102.7452	−13.2751	−102.7452	−74.6487
1.8	−74.6487	−51.6556	−74.6487	−102.7452
1.9	−39.2452	−84.9796	−39.2452	−120.7842
2.0	0.0000	−109.9852	0.0000	−127.0000

Data in Table I is used to plot the graph in Figure 8. ia, ib and ic are lagging 120° from each other while ibetha (iβ) leads ialpha (iα) by 90°.

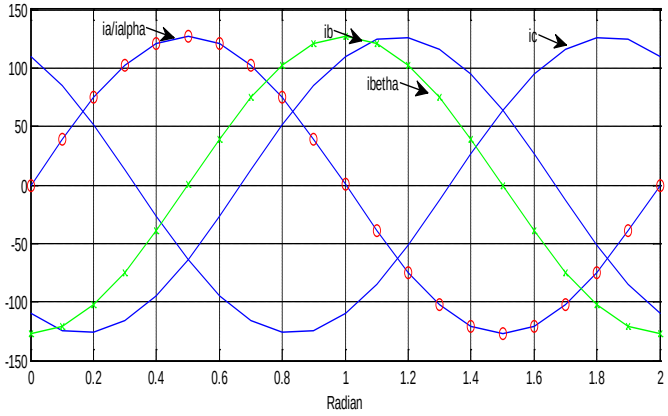

Fig. 4 The desired plot of Clarke transformation

Referring to Figure 5, using an internal Altera DE II clock frequency of 50MHz, the calculation is completed approximately within 4 clock cycles with output error ±1 due to rounding up or down. Besides that there are also visible glitches occurs at every signal transition at duration of less than 10ns. This can be solved by storing the final result in an output register by strobing it after 4 clock cycles.

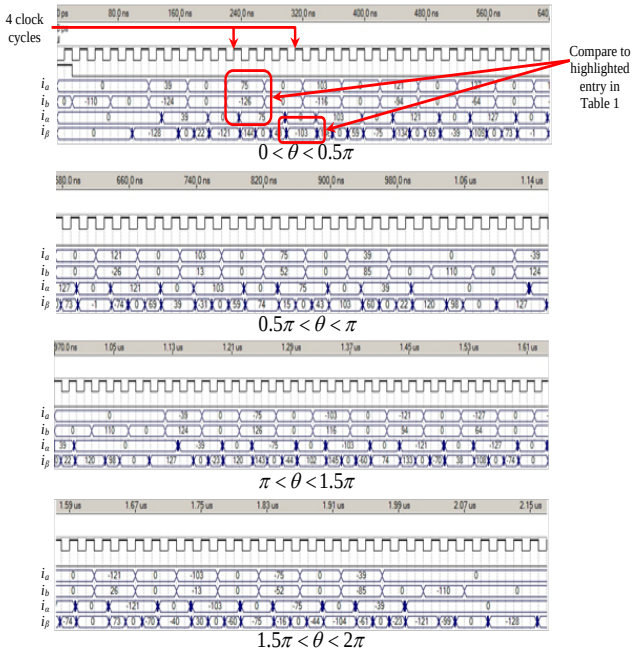

Fig. 5 Timing Simulation Waveform

The actual implementation if the module on a real FPGA had also been done. In Figure 6, the correct functional result of the highlighted entry in Table 1 was successfully obtained on the Cyclone II FPGA of Altera DE II Board.

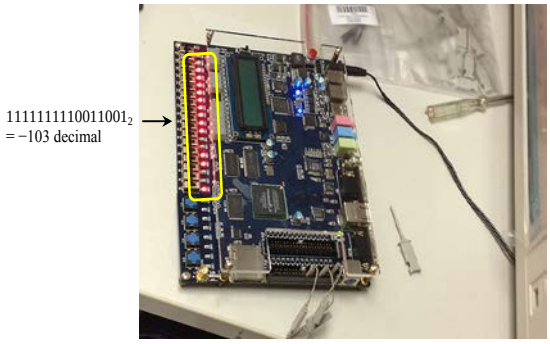

Fig. 6 Functional test on Altera DE II

IV. Conclusion

The hardware implementation of mathematical three phase conversion concept used in Clarke's Transformation that employs space vector concepts had been successful. Simulation proved our implementation was able to perform the calculation in 4 clock cycles. The experiment on a real FPGA showed that the expected functional result was obtained. The real 4 clock cycles timing on the FPGA was also captured on a logic analyzer but that result shall be published for a future paper as it involved a considerable test bench processes and would exceed the space for this paper.

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